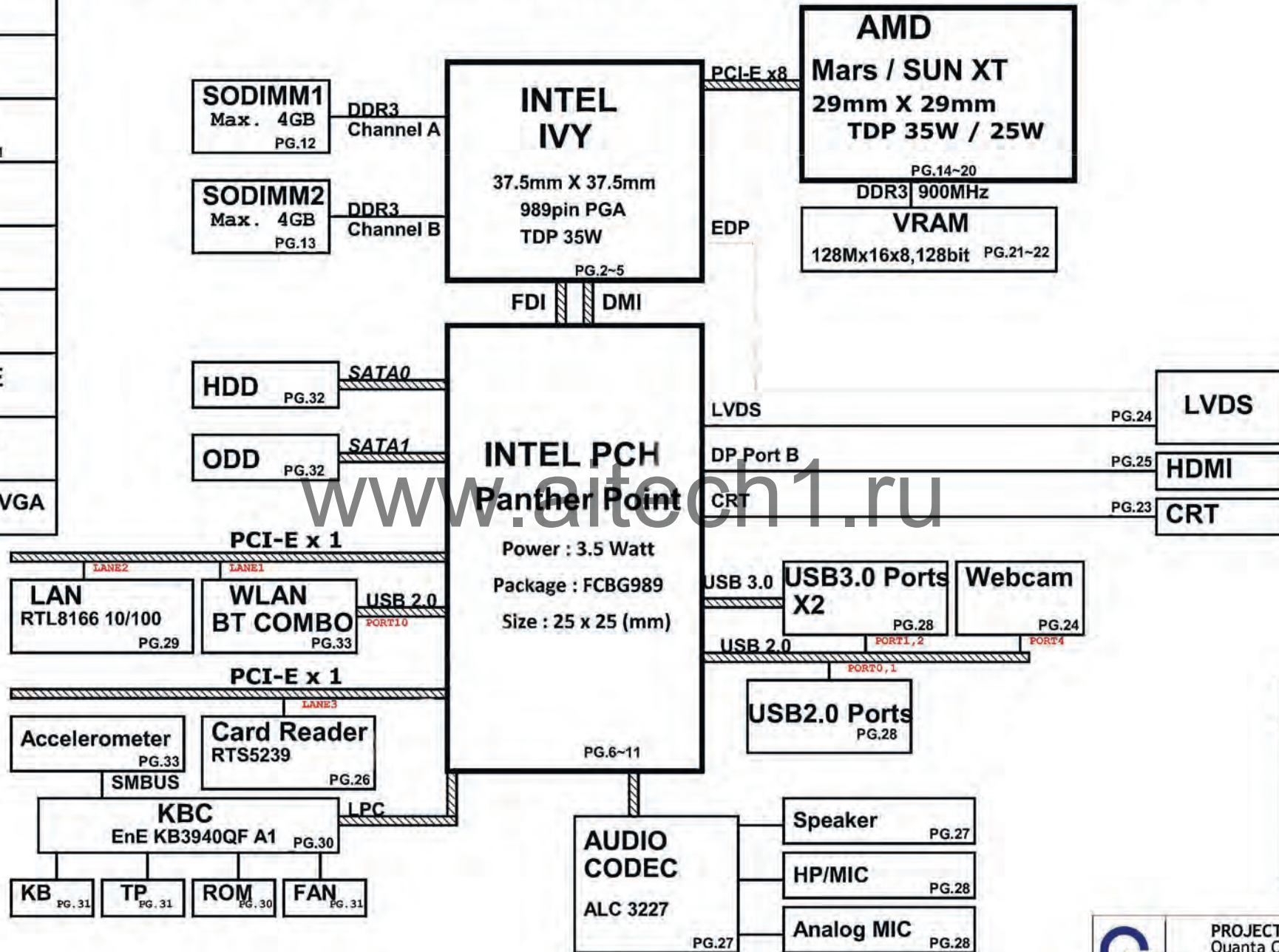


R62 INTEL CHIEF RIVER SYSTEM DIAGRAM

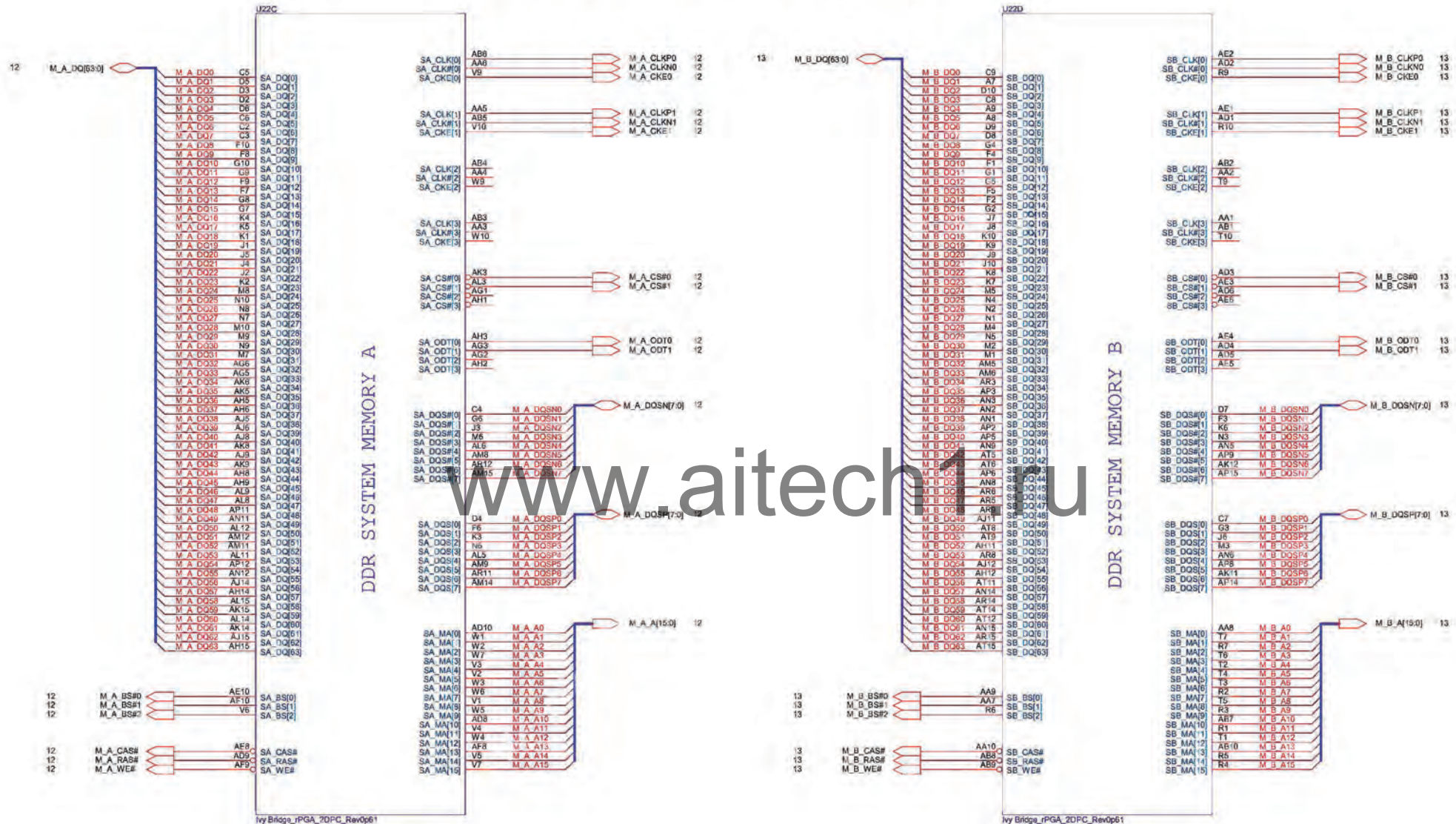
01

+3V/+5V S5
PG.35
+1.05V
PG.36
CPU Core
PG.40~41
DDR3
PG.37
Charge
PG.34
Dis-Charge
PG.39
+VGACORE
PG.42
+VCCSA
PG.38
+1.0V/+1.8/ +3 VGA
PG.43





Ivy Bridge Processor (DDR3)



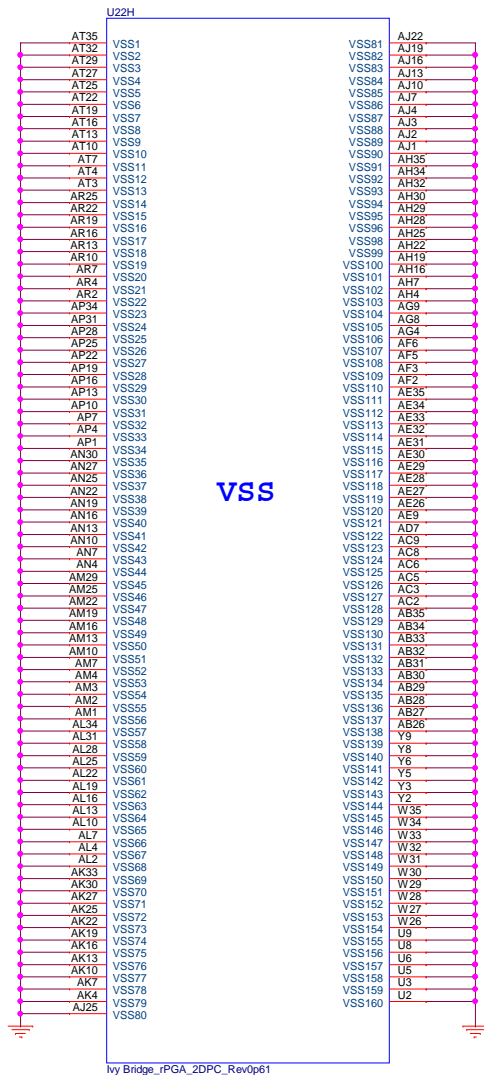
04

POWER

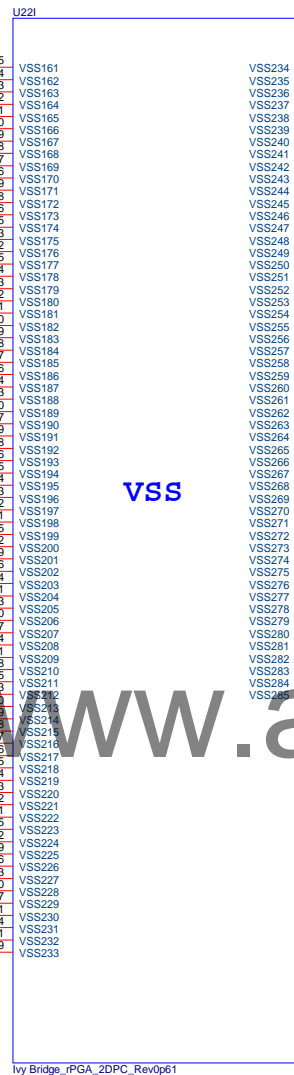


Size Custom	Document Number SNB 3/4 (POWER)	Re
Date: Monday, October 22, 2012	Sheet 4 of 43	

Ivy Bridge Processor (GND)



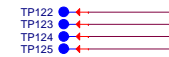
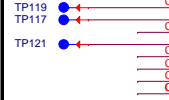
Ivy Bridge_rPGA_2DPC_Rev0p61



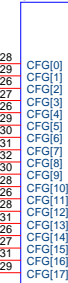
Ivy Bridge_rPGA_2DPC_Rev0p61

Ivy Bridge Processor (RESERVED, CFG)

For CPU debug.

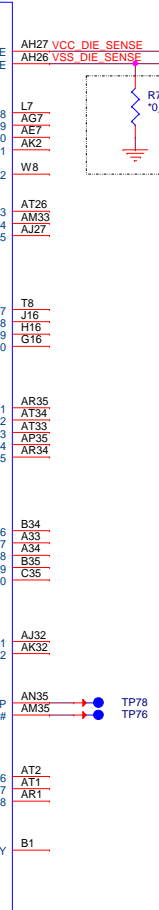


U22E



CFG

RESERVED



For rPGA socket, RSVD59 pin should be left NC.

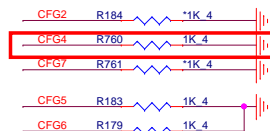
CFG[6:5] (PCIe Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

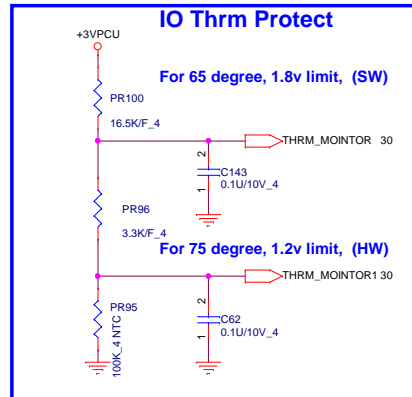
	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



IO Thrm Protect

For 65 degree, 1.8v limit, (SW)

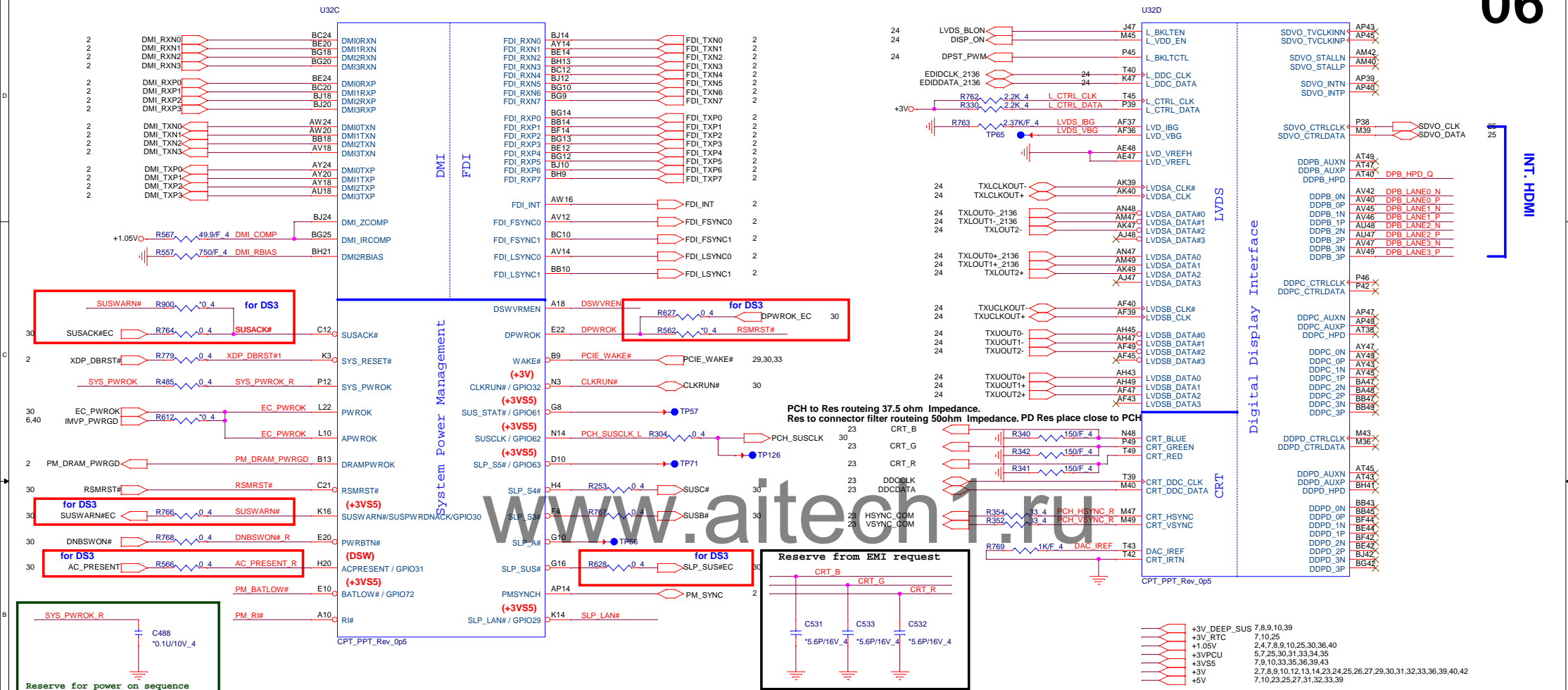
For 75 degree, 1.2v limit, (HW)



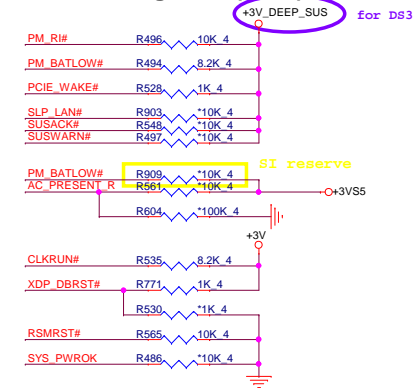
Cougar Point/Panther Point (DMI,FDI,PM)

Cougar Point/Panther Point (LVDS,DDI)

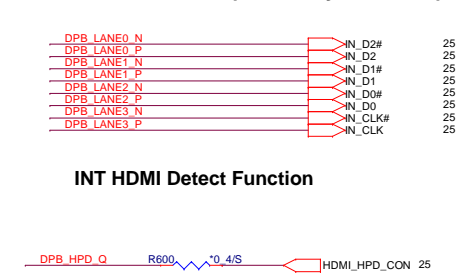
06



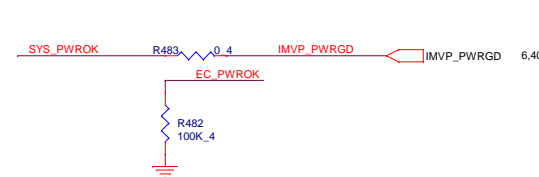
PCH Pull-high/low(CLG)



INT HDMI disable (DIS only remove)



System PWR_OK(CLG)



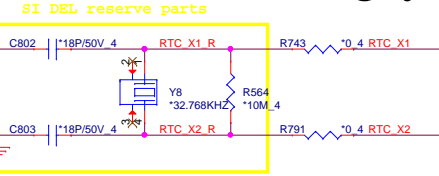
PROJECT : R62
 Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 1/6 (DMI/FDI/VIDEO)	1A
Date: Monday, October 22, 2012	Sheet 6	of 43

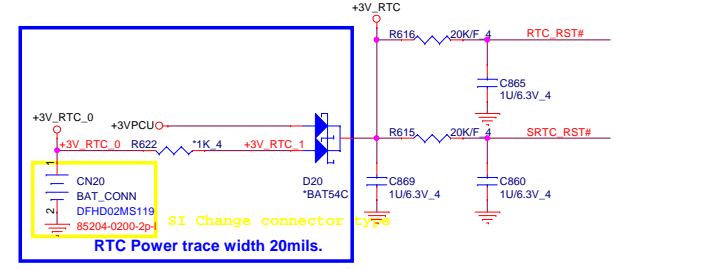
Cougar Point/Panther Point (HDA,JTAG,SATA)

07

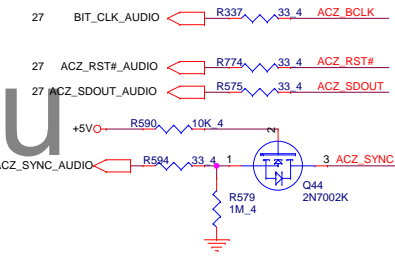
RTC Clock 32.768KHz



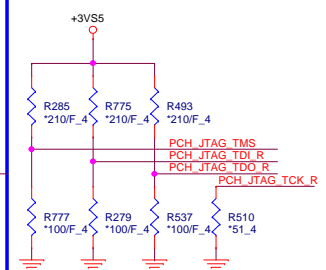
RTC Circuitry(RTC)



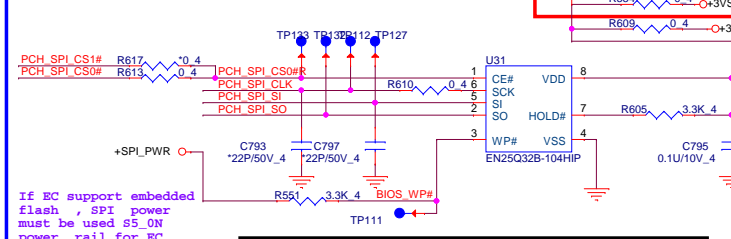
HDA Bus(CLG)



PCH JTAG Debug(CLG)



PCH SPI ROM(CLG)



Vender	Size	P/N
EON	4MB	AKE39ZN0Q02 (EN25Q32B-104HIP)
PMC	4MB	AKE39ZN0500 (PM25LQ032C-BCE)
AMIC	4MB	AKE39F-0800 (A25LQ32AM-F/Q)
Socket		DFHS08FS023

PROJECT : R62
Quanta Computer Inc.

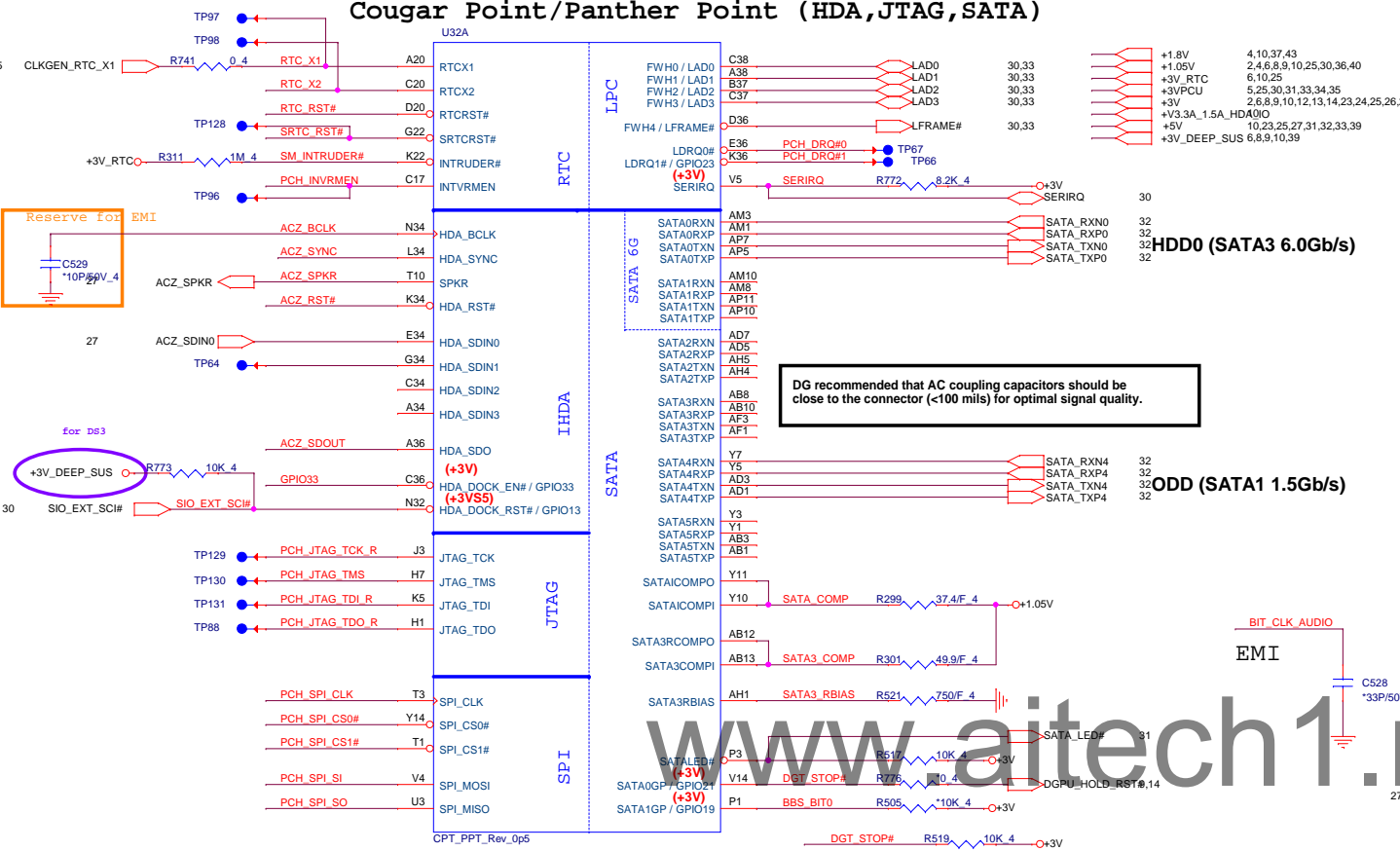
Size Custom

Document Number PCH 2/6 (SATA/HDA/SPI)

Date: Monday, October 22, 2012

Rev 1A

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PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	Different from Calpella No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V ₀ R595 10K 4 PCI_GNT3# 8
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	PCH_INVTRMEN R563 330K 4 +3V ₀ RTC
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	GPIO33 R572 0 4 BIOS_WP#
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1# R782 1K 4 BBS_BIT0 R595 1K 4 BBS_BIT1 8
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK		
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V ₀ R783 1K 4 NV_ALE 8
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V ₀ R526 2.2K 4 R546 1K 4 NV_CLE H_SNB_IVB# 9
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+V3.3A_1.5A_HDA_IO 0 R784 1K 4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Overridden	GPIO33_E ACZ_SDOUT R573 1K 4 +V3.3A_1.5A_HDA_IO
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	
SPI_MOSI	ITPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	

DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

ODD (SATA1 1.5Gb/s)

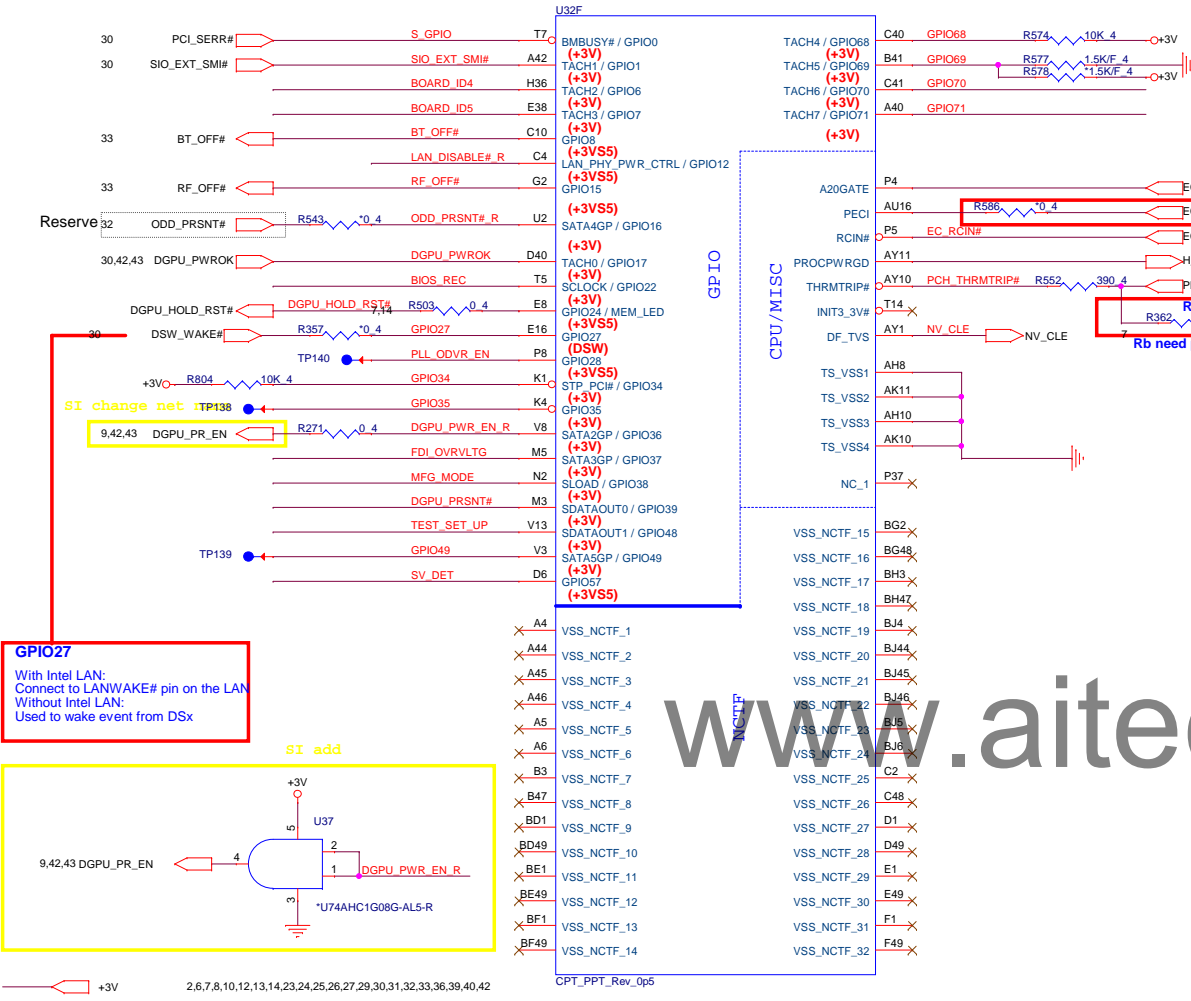
EMI

C528 *33P/50V_4

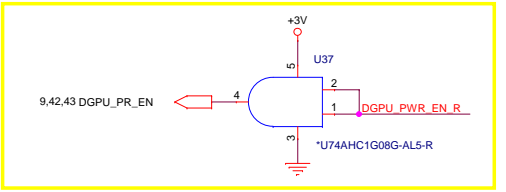
DGT_STOP# R519 10K 4 +3V

+3V

Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)



GPIO27
With Intel LAN:
Connect to LANWAKE# pin on the LAN
Without Intel LAN:
Used to wake event from DSx



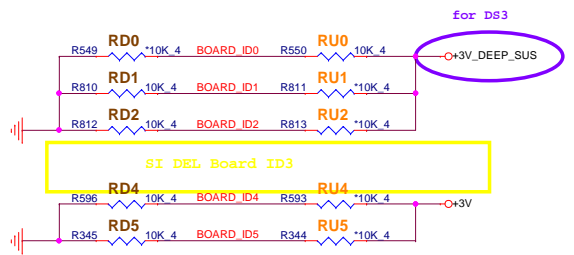
SI add

BOARD ID SETTING

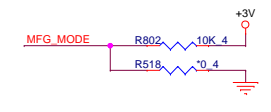
Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
DB R62 UMA				0	0	0
DB R62 DIS				0	0	1
				0	1	1
			1	1	1	1
			0	0	0	0

BOARD_ID1
For Stage Use

BOARD_ID0 BOARD_ID0 8
BOARD_ID1 BOARD_ID1 8
BOARD_ID2 BOARD_ID2 8

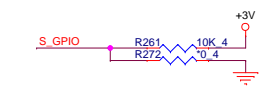


MFG-TEST



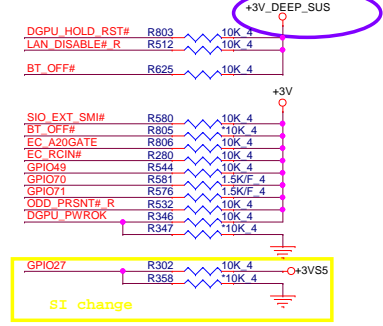
Swap GPIO

0 = SGPIO
1 = Default

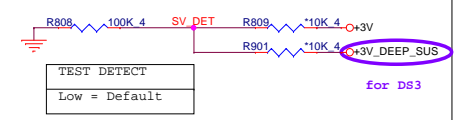
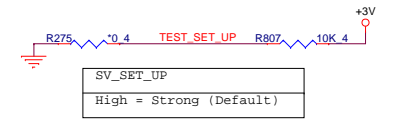
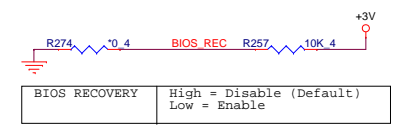


for DS3

GPIO Pull-up/Pull-down(CLG) for DS3

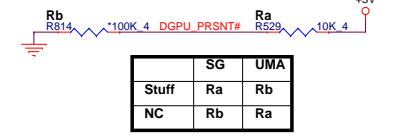


Intel ME Crypto Transport Layer
Security (TIS) cipher suite
Low = Disable (Default)
High = Enable



for DS3

GFX Present



SG	UMA
Stuff	Ra Rb
NC	Rb Ra

PROJECT : R62
Quanta Computer Inc.

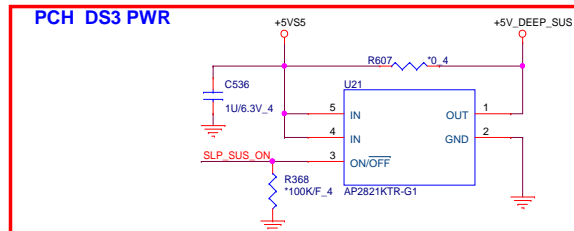
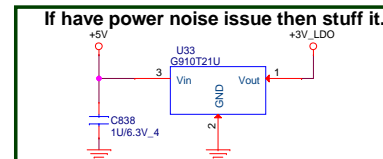
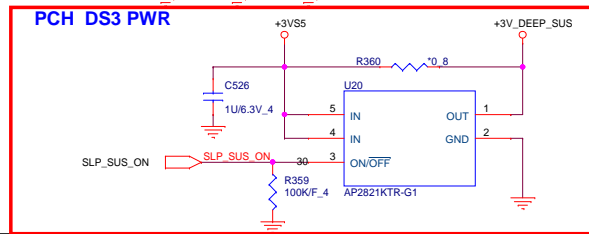
Size Custom	Document Number PCH 4/6 (GPIO/MISC)	Rev 1A
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POWER



1.3 A (60mils)

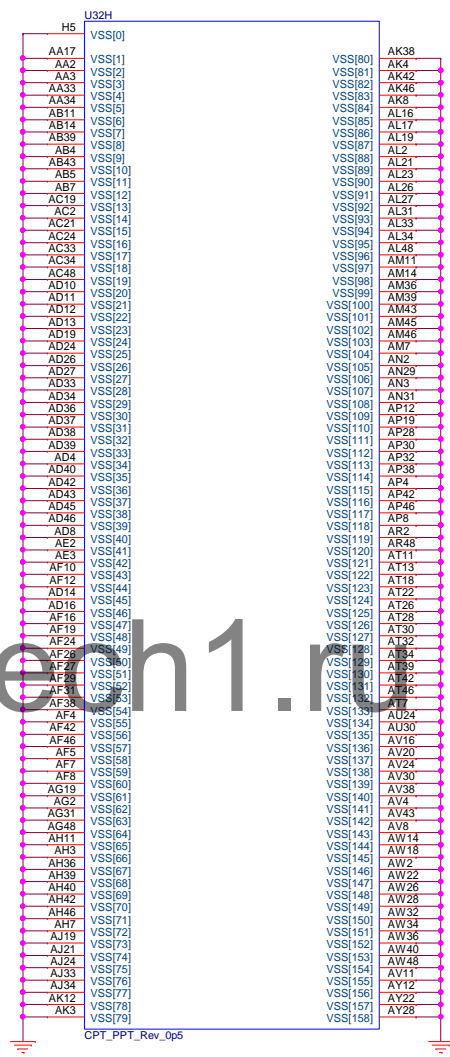
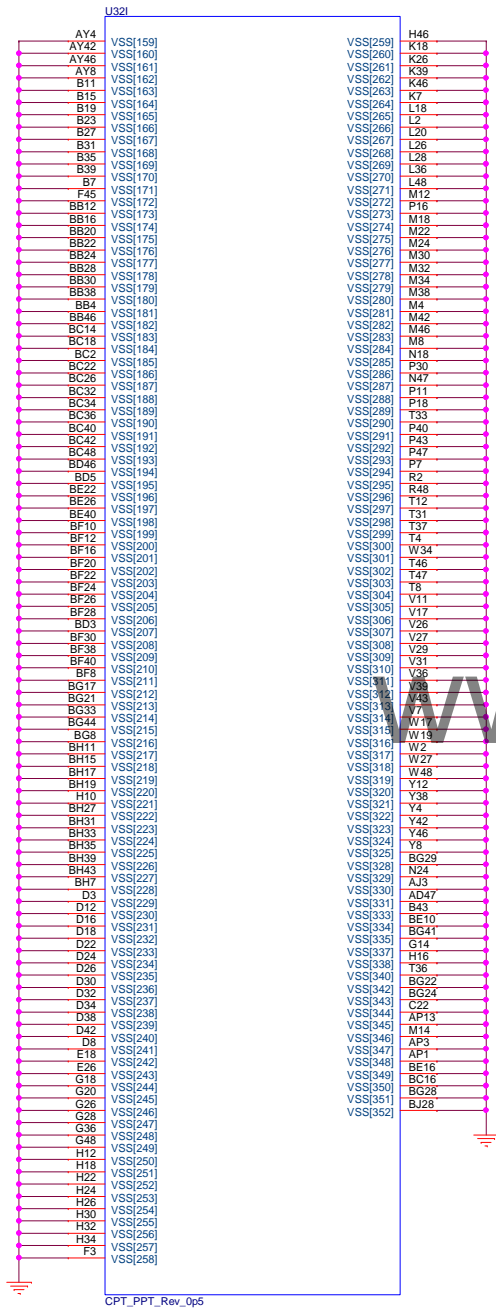
10

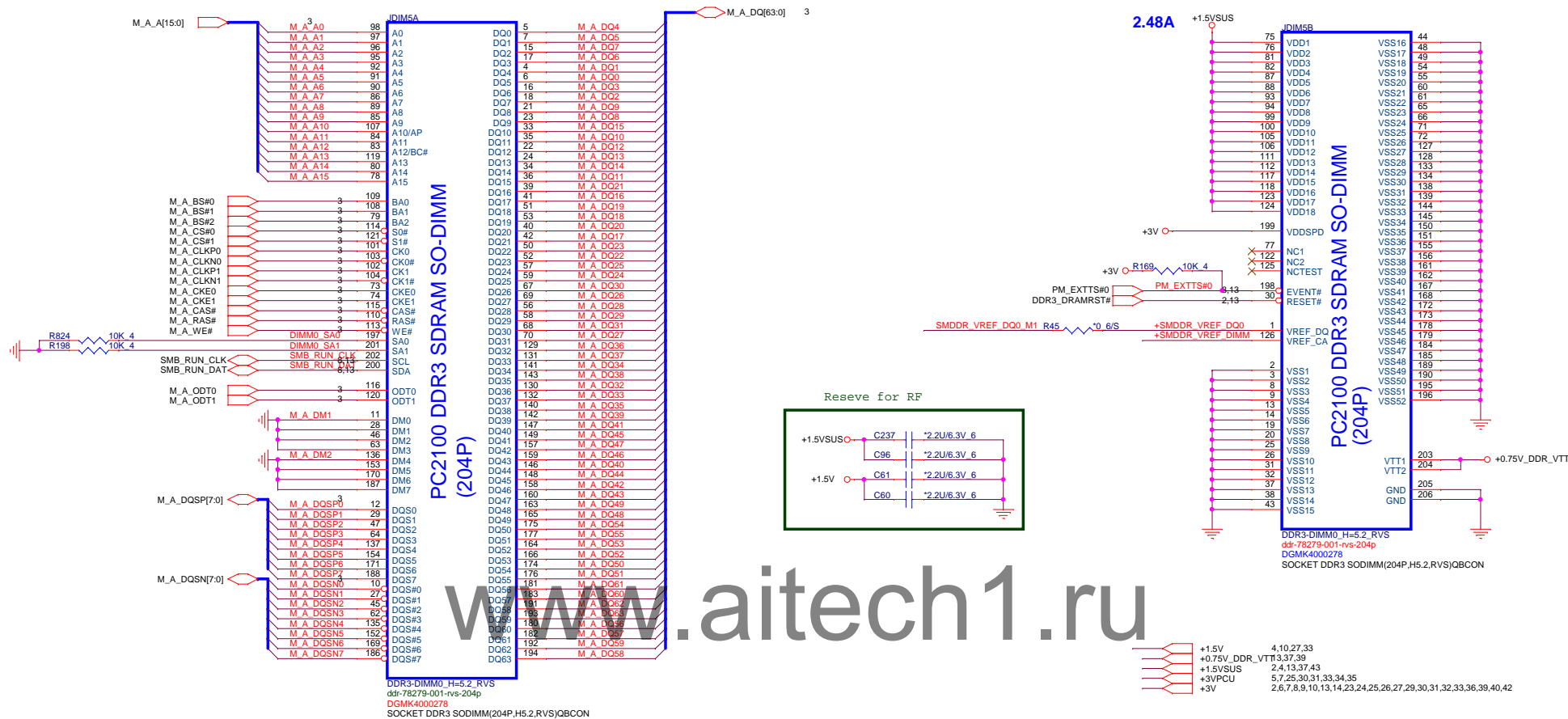


	PROJECT : R62 Quanta Computer Inc.		
	Size Custom	Document Number PCH 5/6 (POWER)	Rev 1A
	Date: Monday, October 22, 2012 Sheet 10 of 43		

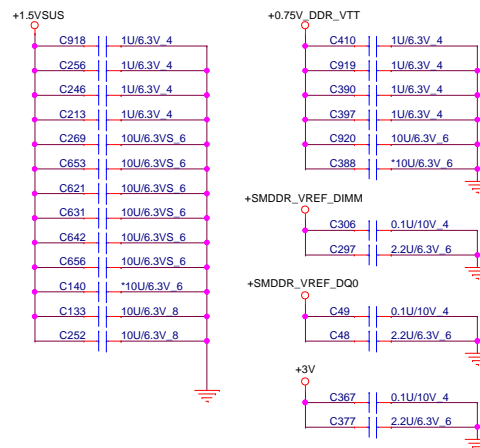
Cougar Point/Panther Point (GND)

Cougar Point/Panther Point (GND)

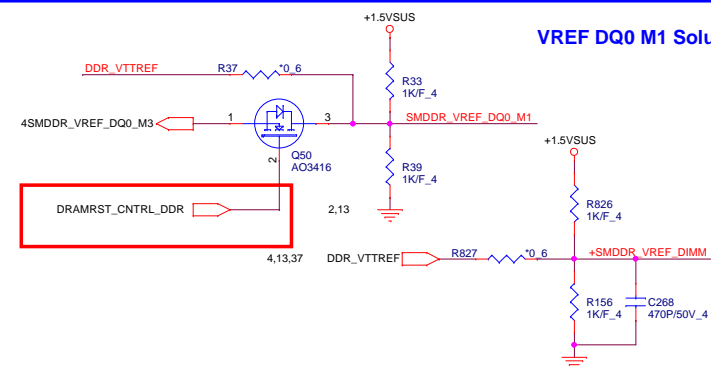


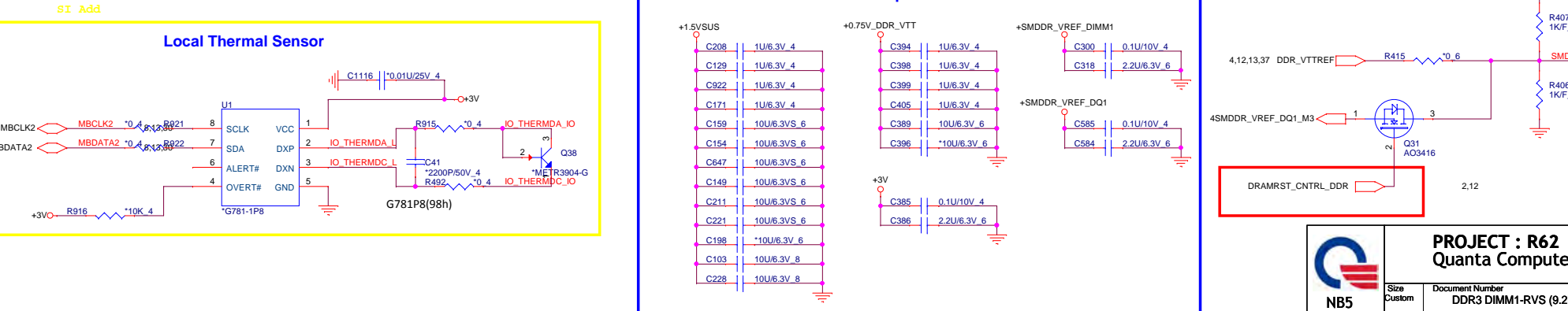


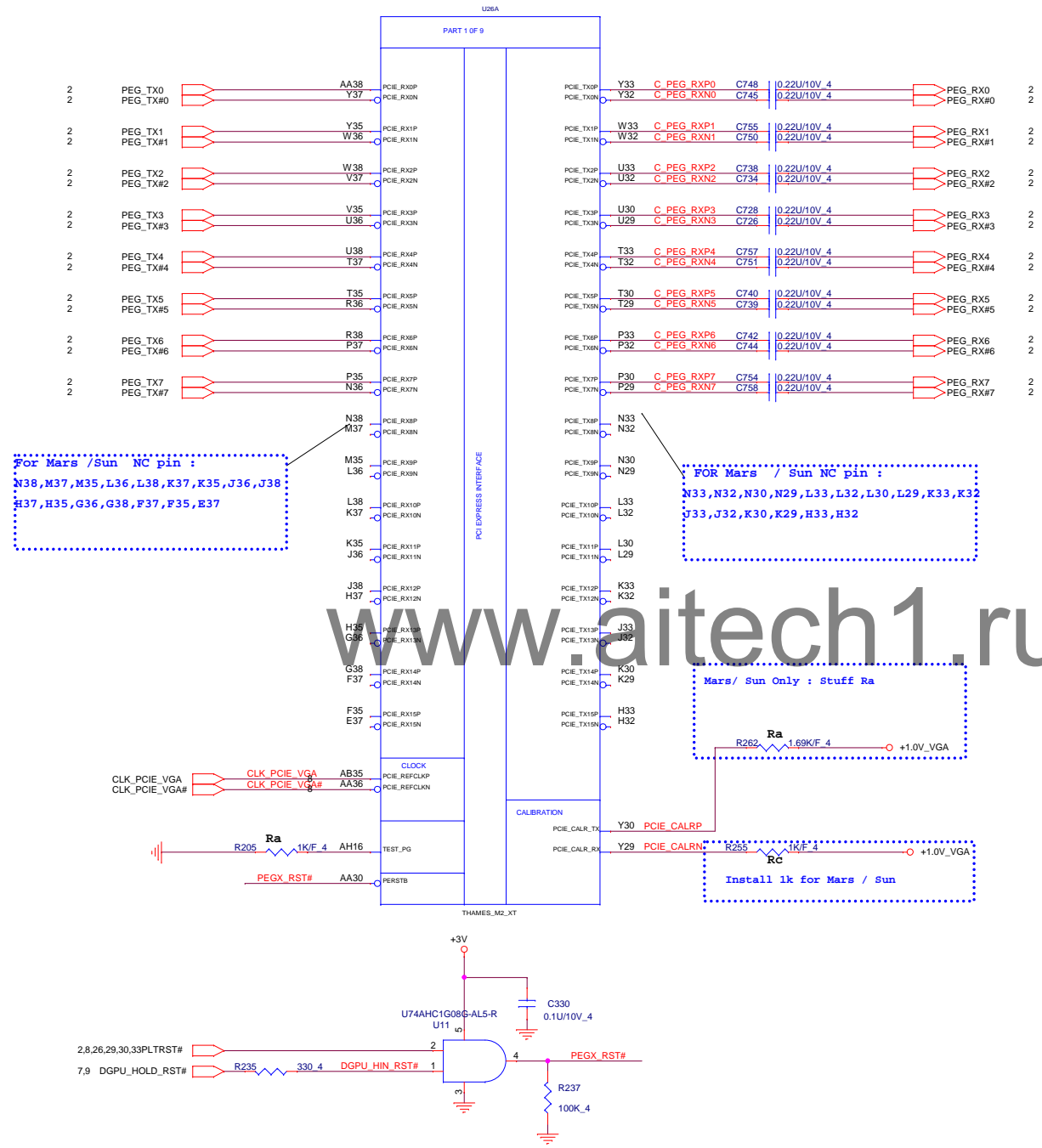
Place these Caps near So-Dimm0.



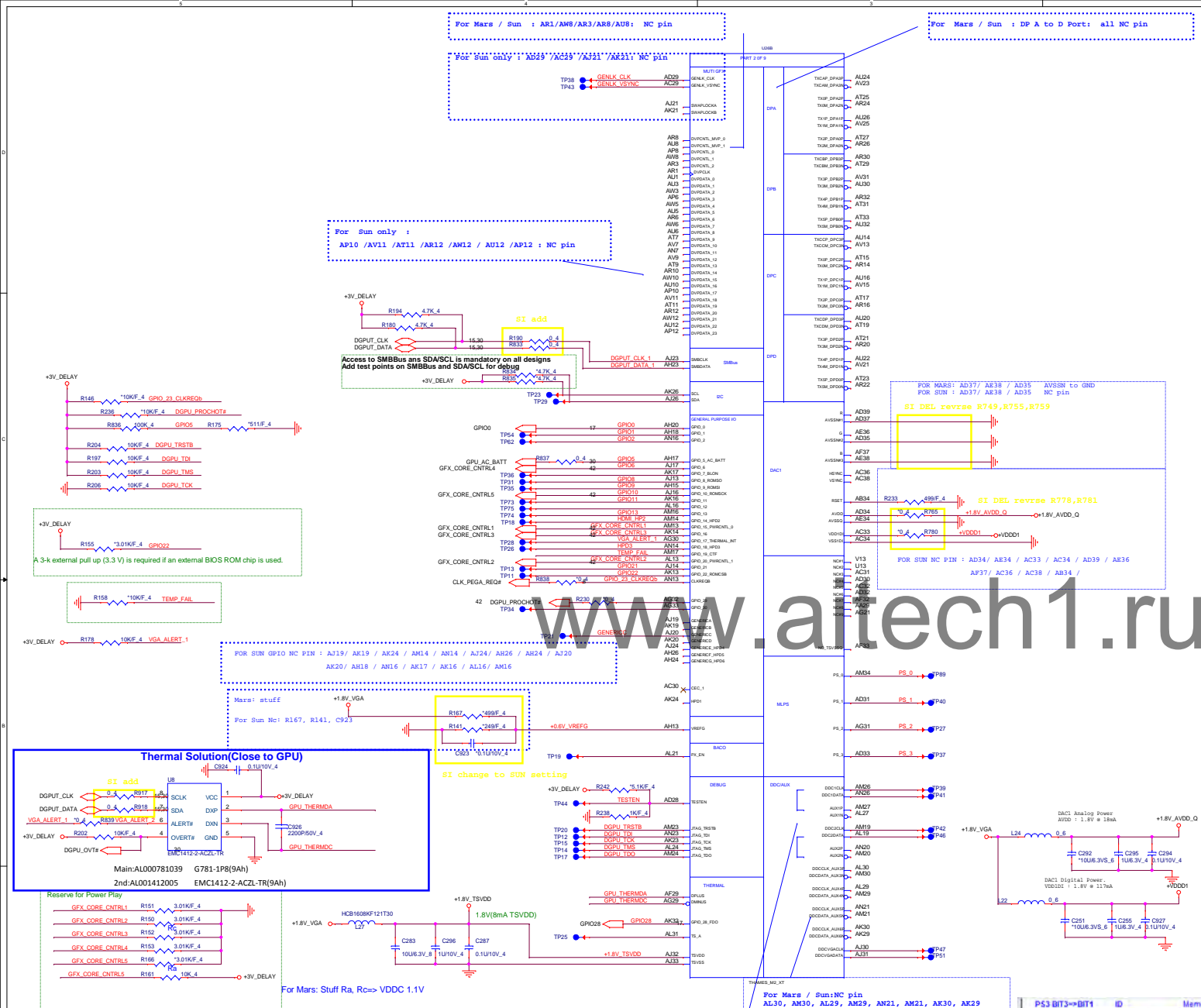
VREF DQ0 M1 Solution







2,6,7,8,9,10,12,13,23,24,25,26,27,29,30,32,33,36,39,40,42
16,18,19,43 +1.0V_VGA



MLPS Implementation

- Connect GPIO_28 to 10K pulldown to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_pu, R_pd and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

R_pu (Ohm)	R_pd (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Pin/Bit	Name	Description	Default	Legacy
PS_0[3:1]	romddg[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romddg[2:0] define memory aperture size If bios_rom_en = 1, romddg[2:0] define ROM type	xxx	gpo_13 gpo_12 gpo_11
PS_0[4]	n/a	Reserved	1	genk_vsync
PS_1[1]	bif_gen0_en_a	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpo_2
PS_1[2]	bif_clk_pm_en	PCIe Clk PM capability: 1 = CLKREQ# supported	x	gpo_8
PS_1[3]	n/a	Reserved		genk_clk
PS_1[4]	tx_pwr_enb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpo_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=Tx de-emphasis enabled	x	gpo_1
PS_2[1]	n/a	Reserved		n/a
PS_2[2]	n/a	Reserved		n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpo_22
PS_2[4]	vga_ds	VGA disable: 1=Disable this GPU as the system's VGA controller	0	gpo_9
PS_2[5]	n/a	Reserved		n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5]	aud_port_ep[2]	3-bit field indicating number of audio-capable display outputs	xxx	n/a
PS_3[4]	aud_port_ep[1]			
PS_3[5]	aud_port_ep[0]			

BIT5 => BIT1

PS0 => 11001

PS1 => 00001

PS2 => 00000

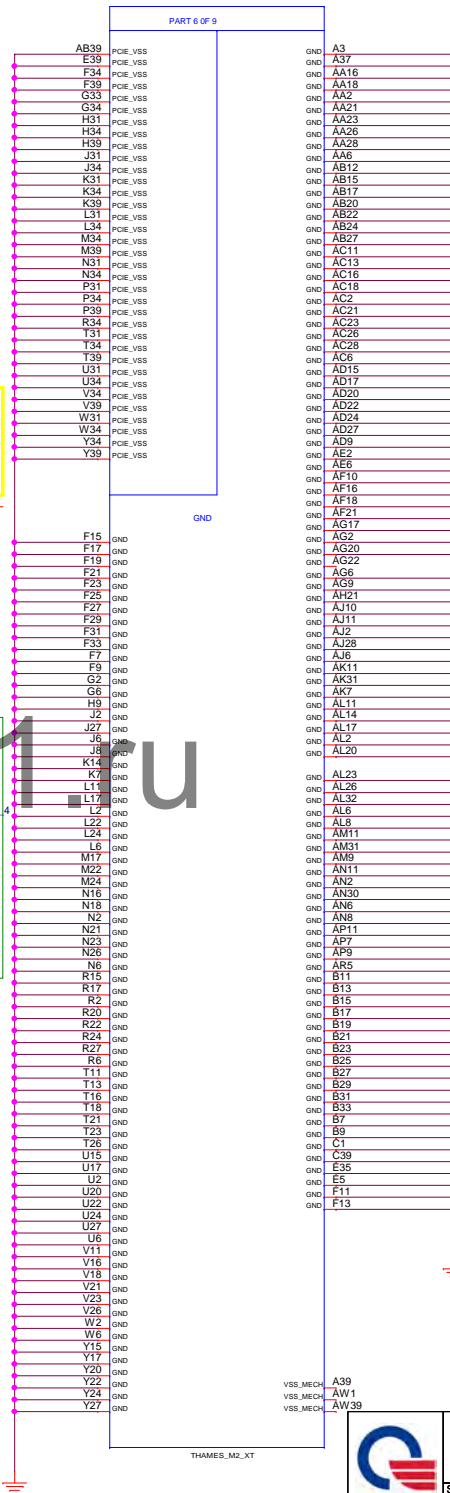
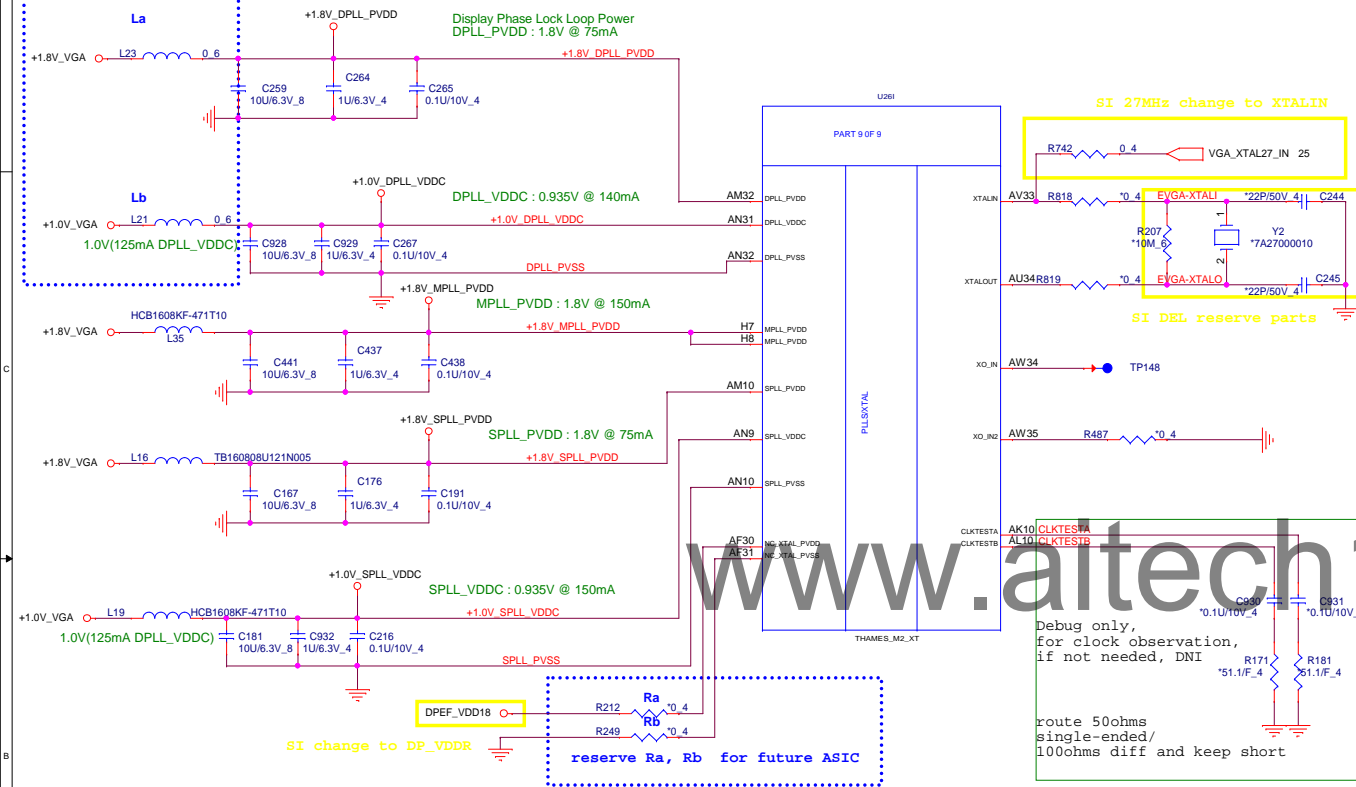
PS3 => 11000

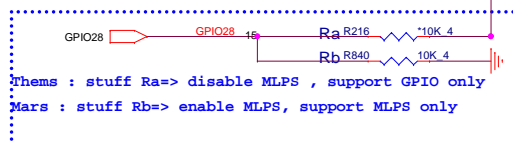
VENDOR	R231	R232
HYNIX 2G	NA	4.75K
MICRON 2G	8.45K	2K
SAM 2G	4.53K	2K
HYNIX 1G	6.98K	4.99K
MICRON 1G	4.53K	4.99K
SAM 1G	3.24K	5.62K

PS3 BIT5 => BIT1	ID	Memory Type	Configuration	PN	Channel Size
000	0	Hynix	H5TC4G63AFR-11C	AKD5P0WTW08 IC SDRAM/96PH5TC4G63AFR-11C	2G
001	1	Micron	MT41J256M10HA-093GE	AKD5P23T101 IC SDRAM/96PMT41J256M10HA-093GE	2G
010	2	Samsung	K4W4G1646B-HC1A	AKD5P2D1T03 IC SDRAM/96PK4W4G1646B-HC1A	2G
011	3	Hynix	H5TC2G63FR-11C	AKD5M2D1W03 IC SDRAM/96PH5TC2G63FR-11C	1G
100	4	Micron	MT41J128M16JT-093GE	AKD5M2D1W03 IC SDRAM/96PH5TC2G63FR-11C	1G
101	5	Samsung	K4W2G1646E-BC1A	AKD5M2D1W03 IC SDRAM/96PK4W2G1646E-BC1A	1G

Memory Type	
DDR3	27-MHz (± 30 ppm) crystal connected to XTALIN/XTALOUT, or 27-MHz (1.8 V) oscillator connected to XTALIN.
GDDR5	27-MHz (3.3 V) oscillator connected to XO_IN, and 100-MHz (3.3 V) oscillator connected to XO_IN2. (By default, this clock should not be spread since internal spreading is used.)

For Mars/ Sun
Change La, Lb
Bead to 0 ohm





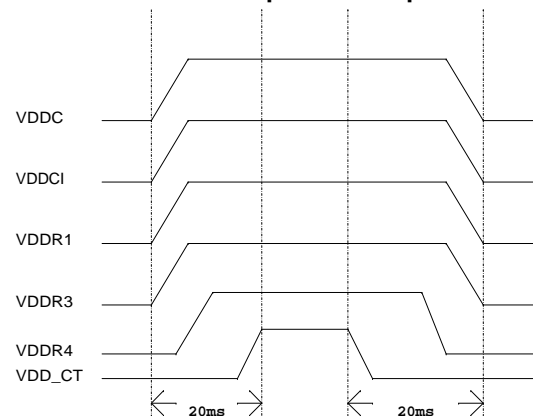
Memory Aperture size

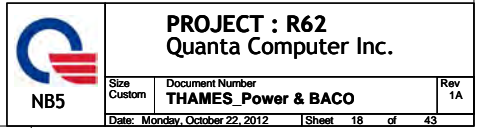
GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

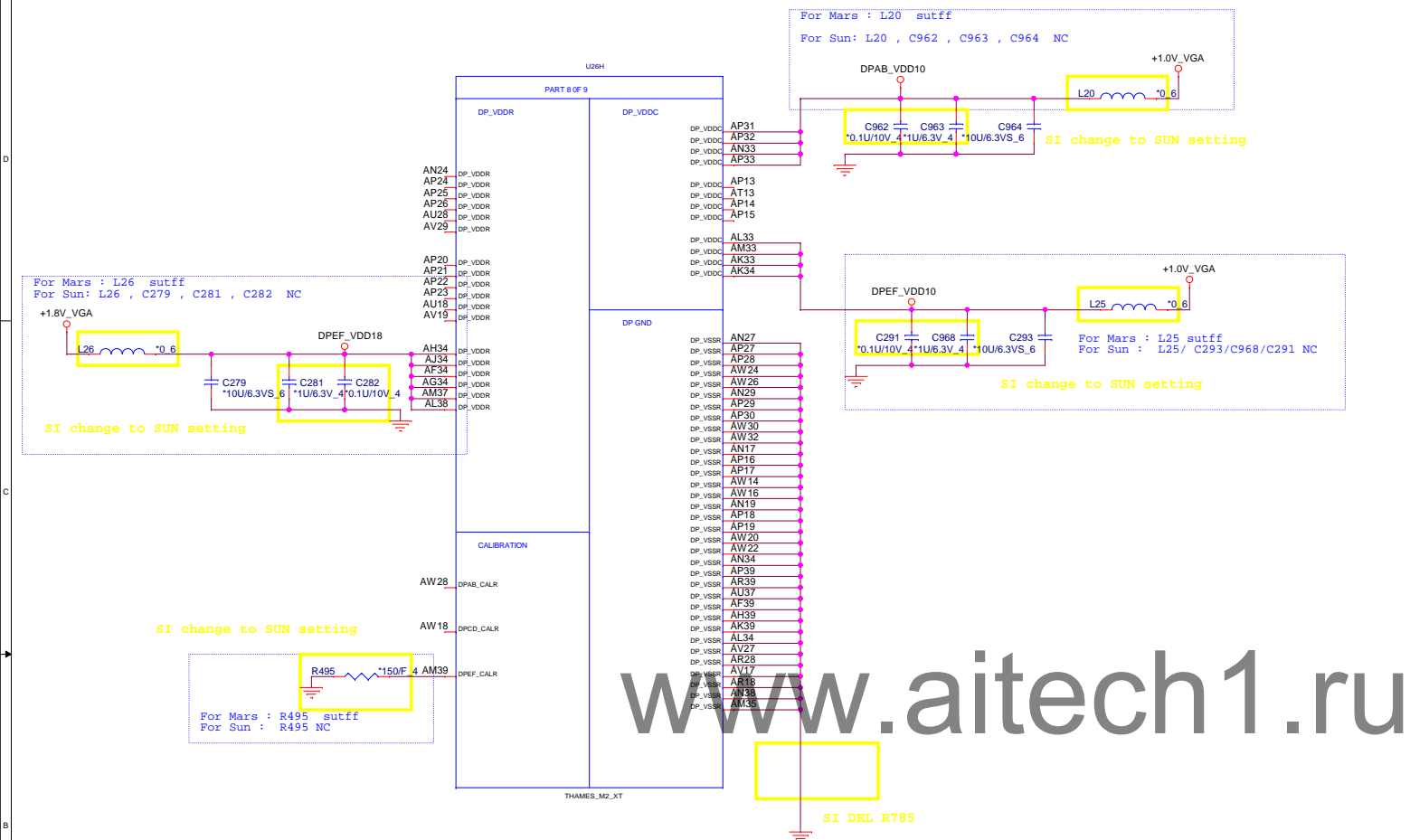
It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET																												
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting																								
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X																								
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X																								
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIe Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X																								
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIe Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1																								
BIF_VGA DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0																								
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type <table><tr><td>100 - 512Kbit</td><td>M25P05A</td><td>(STD)</td></tr><tr><td>101 - 1Mbit</td><td>M25P10A</td><td>(STD)</td></tr><tr><td>101 - 1Mbit</td><td>M25P10A</td><td>(STD)</td></tr><tr><td>101 - 4Mbit</td><td>V25E20</td><td>(STD)</td></tr><tr><td>101 - 4Mbit</td><td>V25E20</td><td>(STD)</td></tr><tr><td>100 - 8Mbit</td><td>M25P80</td><td>(STD)</td></tr><tr><td>100 - 512Kbit</td><td>Fm25LV12</td><td>(Chingis)</td></tr><tr><td>101 - 1Mbit</td><td>Fm25LV10</td><td>(Chingis)</td></tr></table>	100 - 512Kbit	M25P05A	(STD)	101 - 1Mbit	M25P10A	(STD)	101 - 1Mbit	M25P10A	(STD)	101 - 4Mbit	V25E20	(STD)	101 - 4Mbit	V25E20	(STD)	100 - 8Mbit	M25P80	(STD)	100 - 512Kbit	Fm25LV12	(Chingis)	101 - 1Mbit	Fm25LV10	(Chingis)	XXX
100 - 512Kbit	M25P05A	(STD)																										
101 - 1Mbit	M25P10A	(STD)																										
101 - 1Mbit	M25P10A	(STD)																										
101 - 4Mbit	V25E20	(STD)																										
101 - 4Mbit	V25E20	(STD)																										
100 - 8Mbit	M25P80	(STD)																										
100 - 512Kbit	Fm25LV12	(Chingis)																										
101 - 1Mbit	Fm25LV10	(Chingis)																										
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X																								
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX																								
CEC_DIS	PS_0[4]	GENLK_VSYN	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X																								
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOs ARE USED. THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0																								
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] NA PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX																								

Power Up/Down Sequence





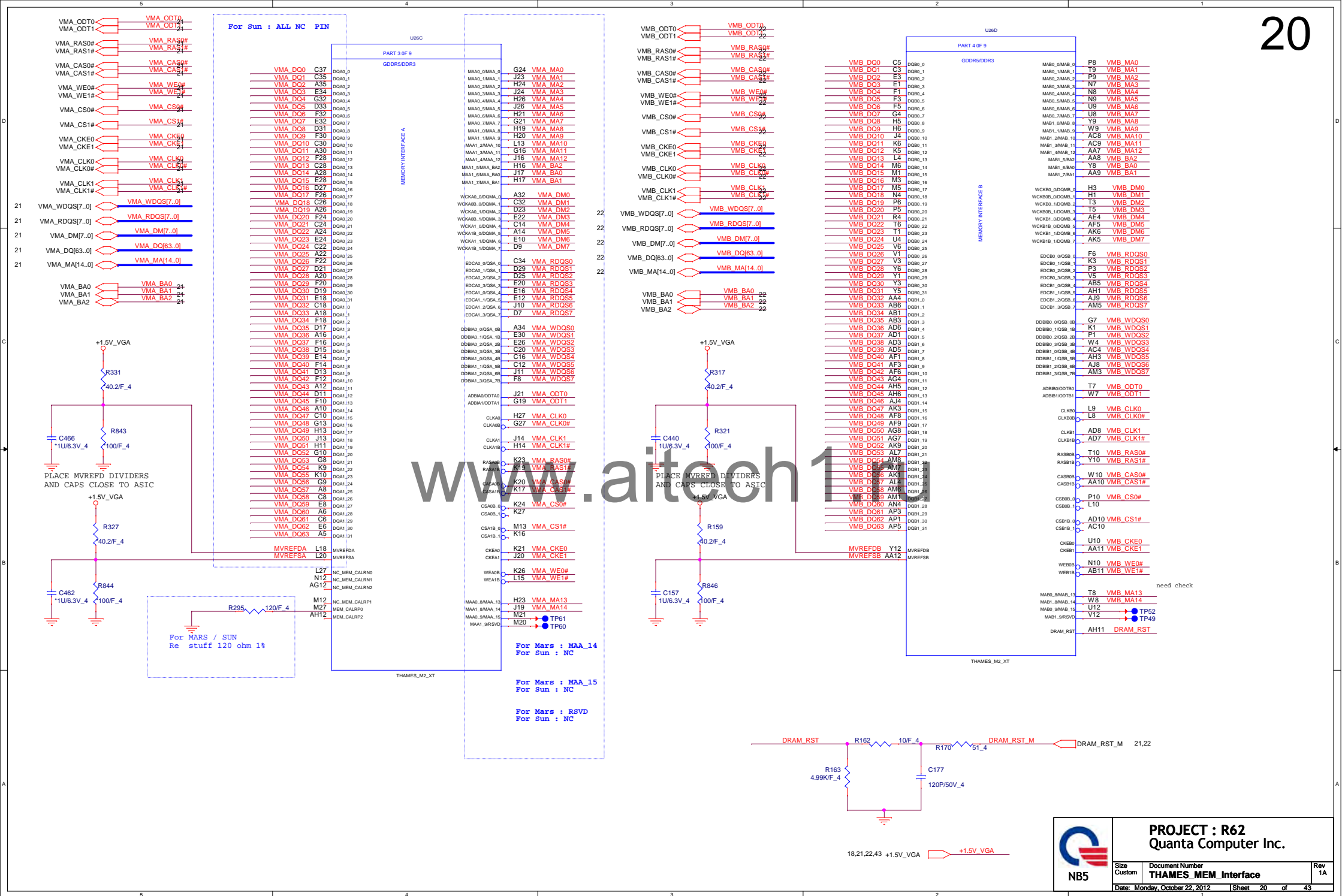


14,16,18,43 +1.0V_VGA
15,16,18,25,40 +1.8V_VGA

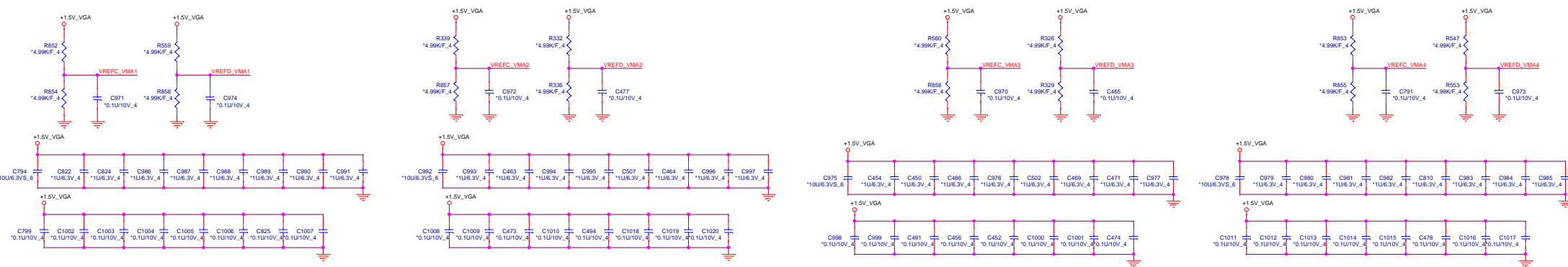
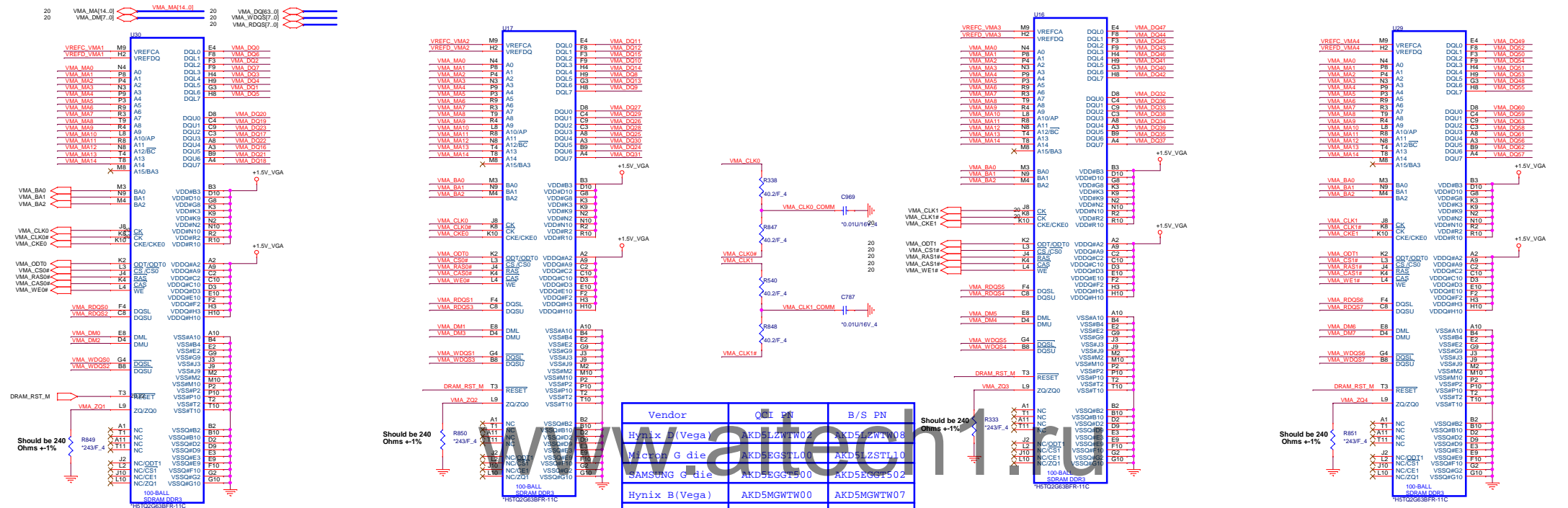


PROJECT : R62
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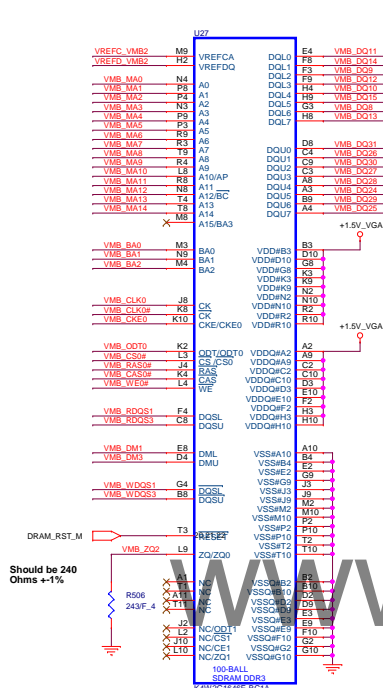
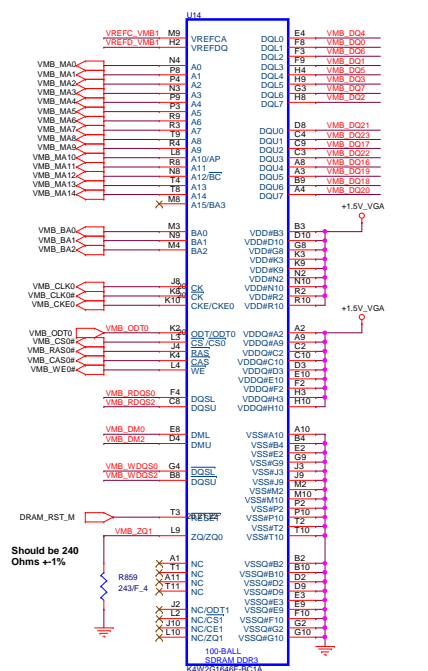
Size	Document Number	Rev
Custom	THAMES_DP Powers	1A
Date: Monday, October 22, 2012 Sheet 19 of 43		



CHANNEL A: 256MB/512MB DDR3

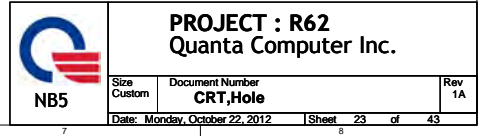


CHANNEL B: 256MB/512MB DDR3

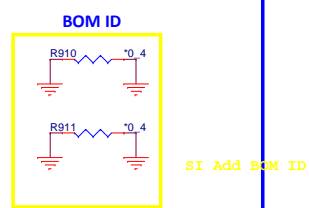
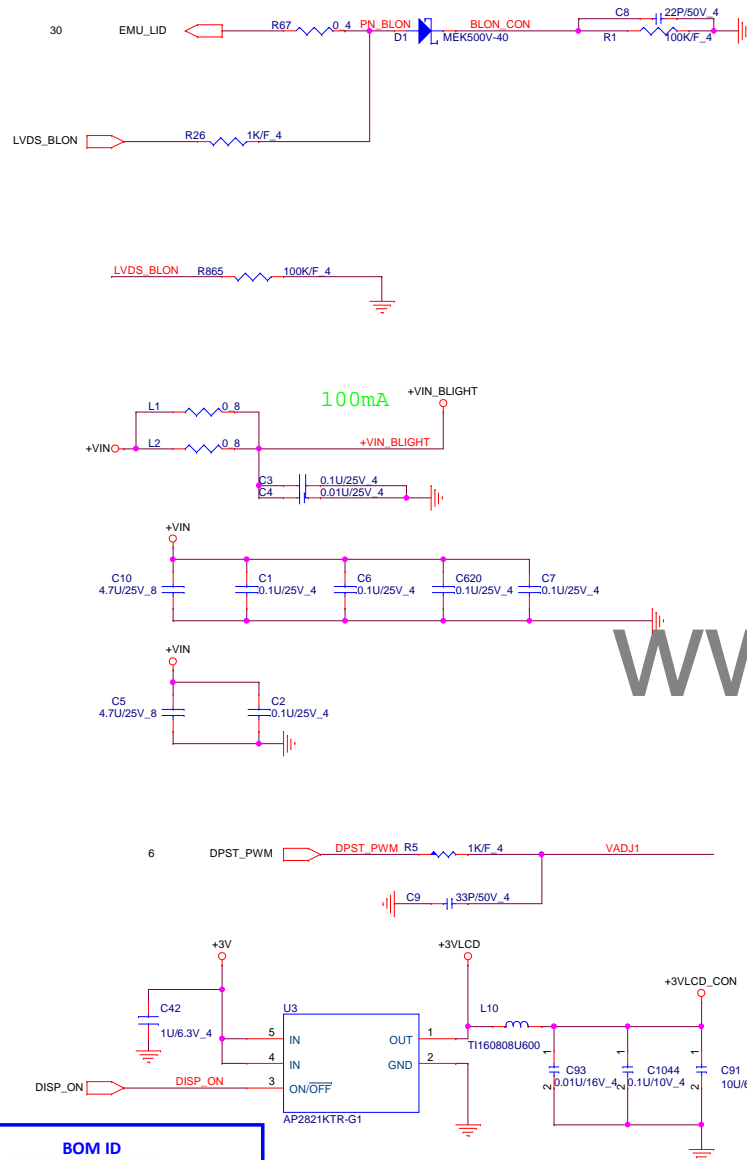




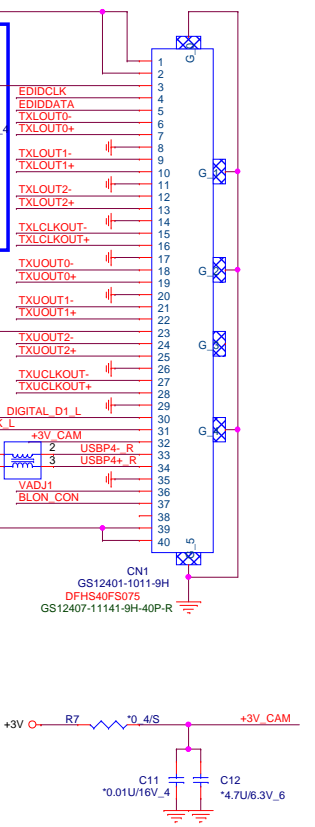
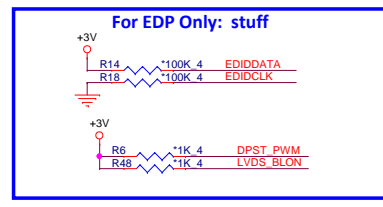
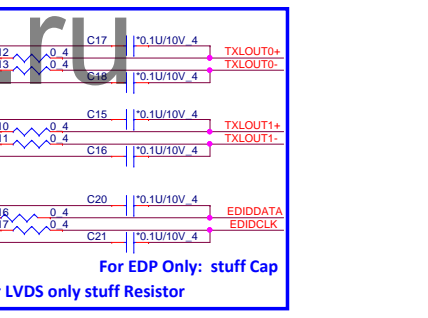
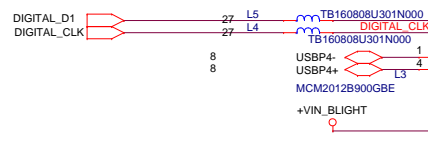
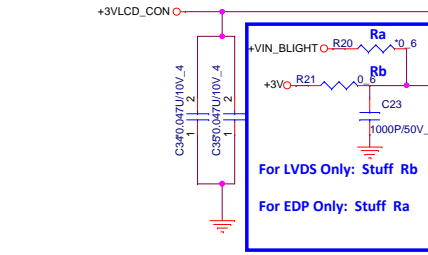
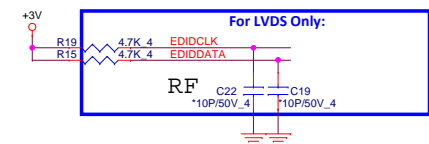
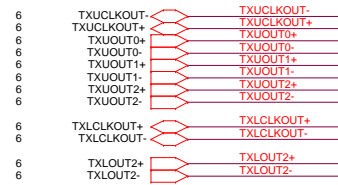
KB lock



LID Switch

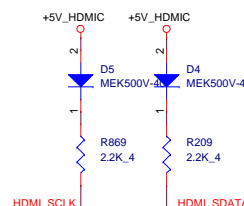
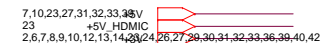


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2,6,7,8,9,10,12,13,14,23,25,26,27,29,30,31,32,33,36,37,5,7,25,30,31,33,34,35,33,34,35,36,37,39,41,42,43

25



8 CLK_PCIE_REQ2# CLK_PCIE_REQ2# R446 0.4/S CLK_PCIE_REQ2#_R

SP1	SD D1	MS D1
SP2	SD D0	MS D0
SP3	SD CLK	MS D0
SP4	SD CMD	MS D0
SP5	SD D3	MS D3
SP6	SD D2	MS CLK
SP7	SD_WP	MS_BS

Share Pin

Close to chip pin

8 CLK_PCIE_CARDP
8 CLK_PCIE_CARDN
8 PCIE_RXP3_CARD
8 PCIE_RXN3_CARD

PCIE_TXP3_CARD
PCIE_TXN3_CARD
C598 0.1U/10V_4
C597 0.1U/10V_4

Please add 9 GND VIAS
connection with thermal PAD

Close to chip pin

SP6 SD D2_R R871 0.4 SD D2
SP5 SD D3_R R443 0.4 SD D3
SP4 SD CMD_R R444 0.4 SD CMD
SP3 DV33_18
SP2 SD CLK_R R441 22.4 SD CLK
SD D0_R R448 0.4 SD D0

Reserve for EMI

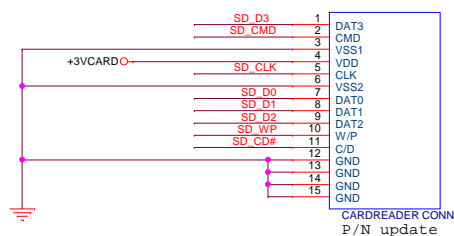
SD D0 C1069 *5.6P/16V_4
SD D1 C612 *5.6P/16V_4
SD D2 C611 *5.6P/16V_4
SD D3 C1068 *5.6P/16V_4

Close to U38

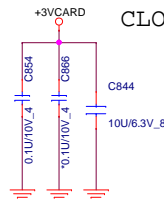
R435 need colse to Chip

SD / MMC

CARD READER
CN8



CLOSE CONN



Reserve for EMI

SD D0 C1049 *5.6P/16V_4
SD D1 C886 *5.6P/16V_4
SD D2 C610 *5.6P/16V_4
SD D3 C1050 *5.6P/16V_4
SD CLK C1100 *5.6P/16V_4

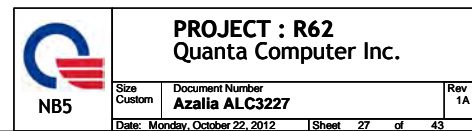
Close to CN8

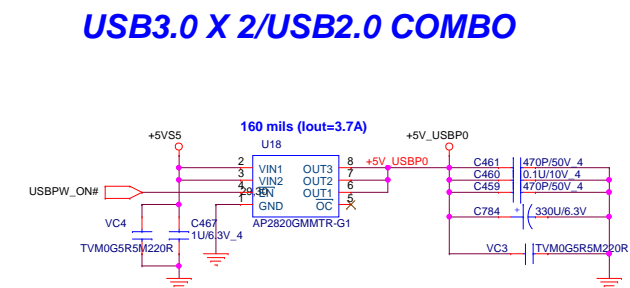
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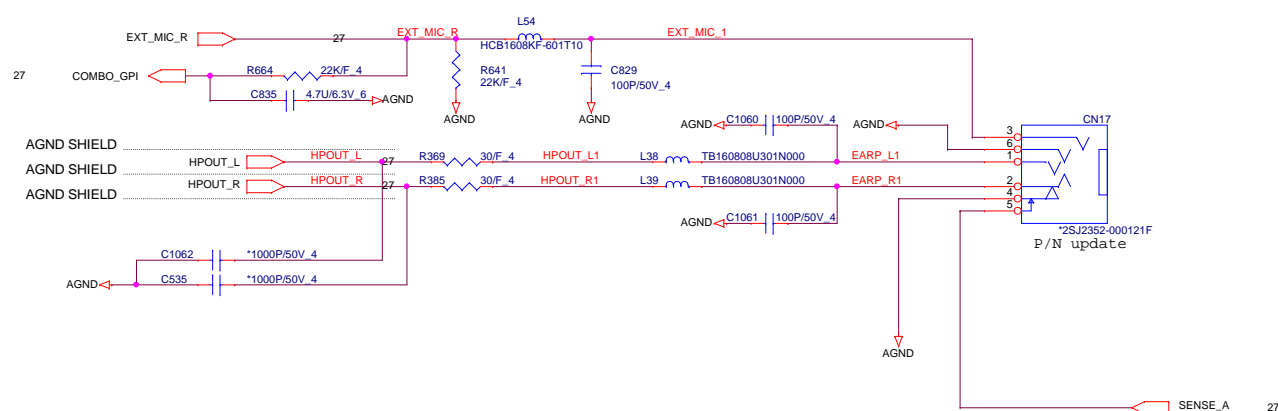
PROJECT : R62
Quanta Computer Inc.

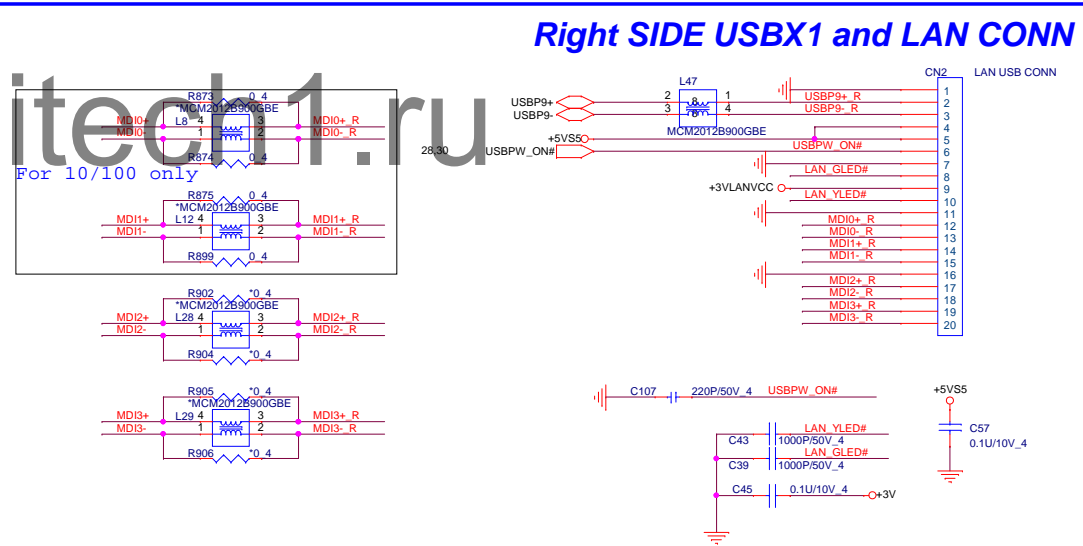
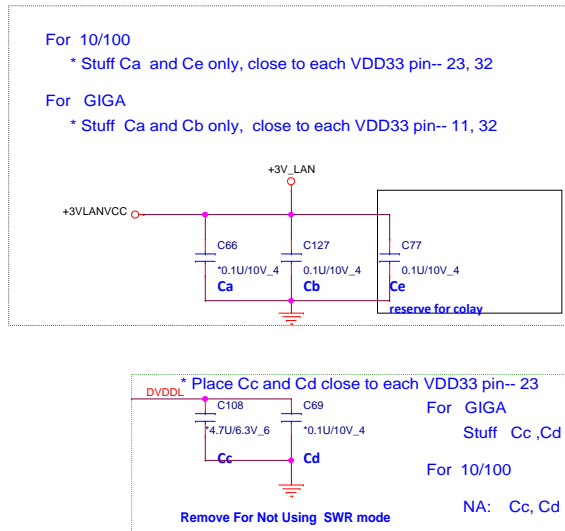
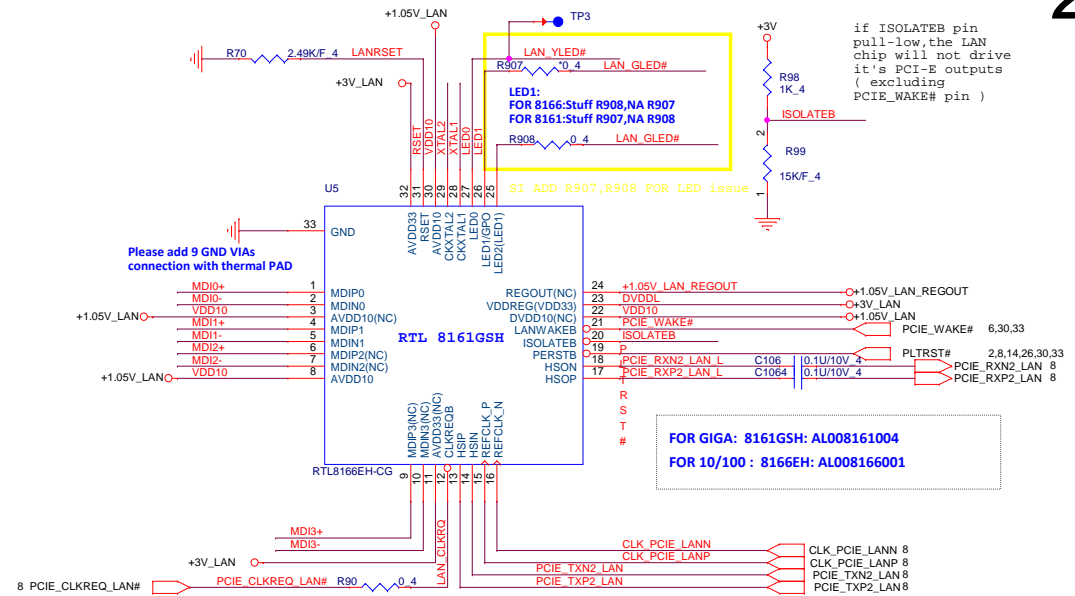
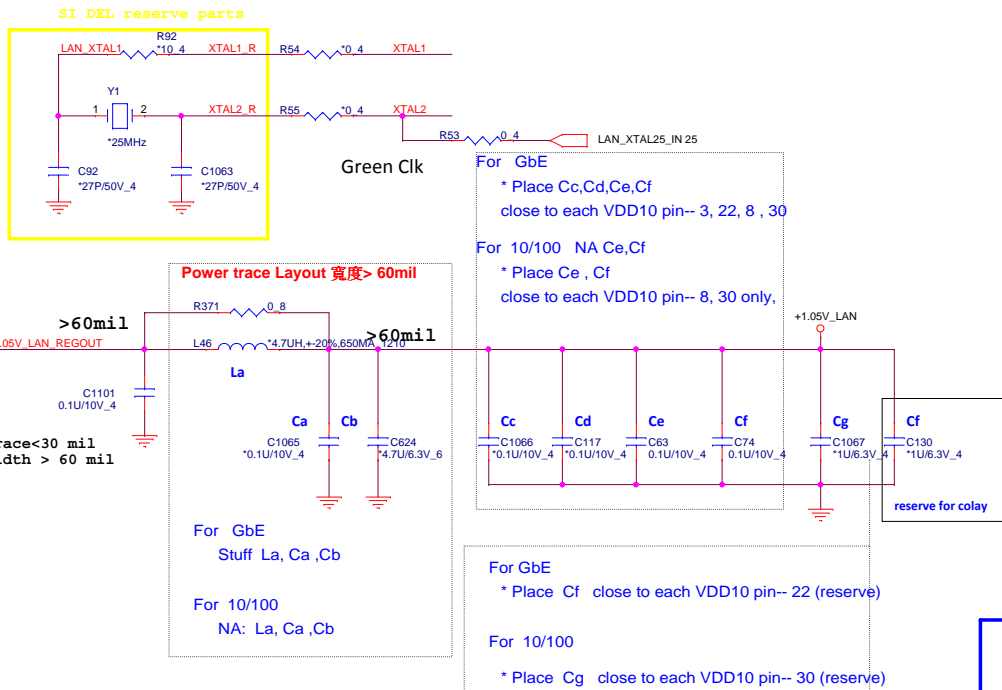
Size Custom	Document Number RTS5229 & CR SOCKET	Rev 1A
Date: Monday, October 22, 2012		Sheet 26 of 43



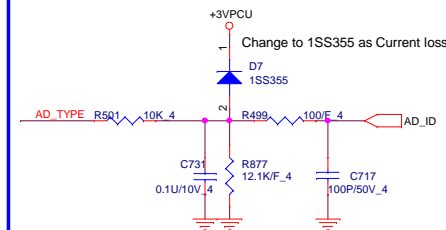


10,29,33,35,36,37,38,39,40,41,42,43
2,6,7,8,9,10,12,13,14,23,24,25,26,27,29,30,31,32,33,36,39,40,42
25,29,39 +3VLANVCC

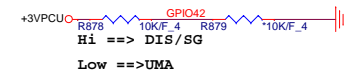




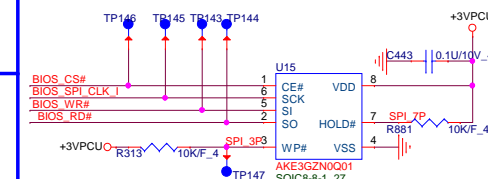
adapter Type check



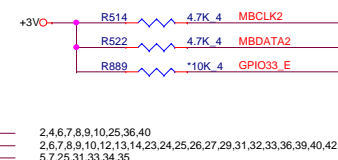
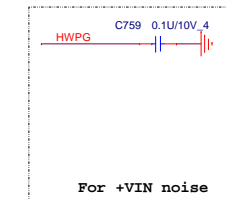
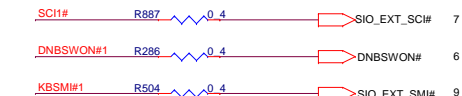
adapter select for EC



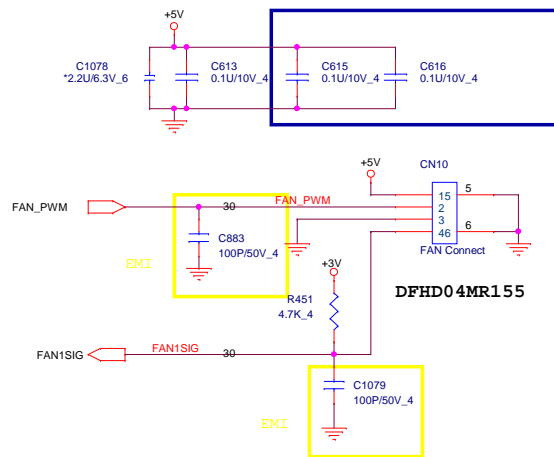
1M byte SPI EC ROM



Vender	Size	P/N
EON	1MB	AKE3GZN0Q01 (EN25Q80A-100HIP)
GigaDevice	1MB	AKE3GGN0Q00 (GD25Q80BSIGR)
AMIC	1MB	AKE3GZP0801 (A25L080M-F)
Socket		DFHS08FS023

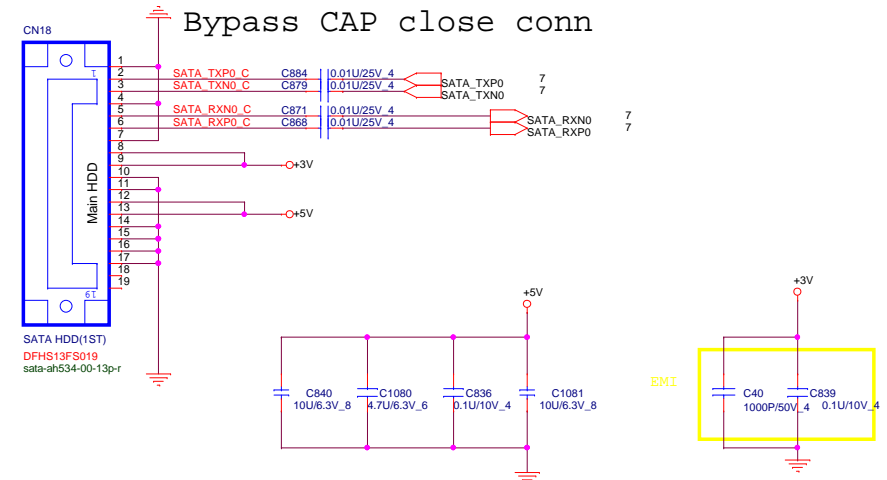


CPU FAN

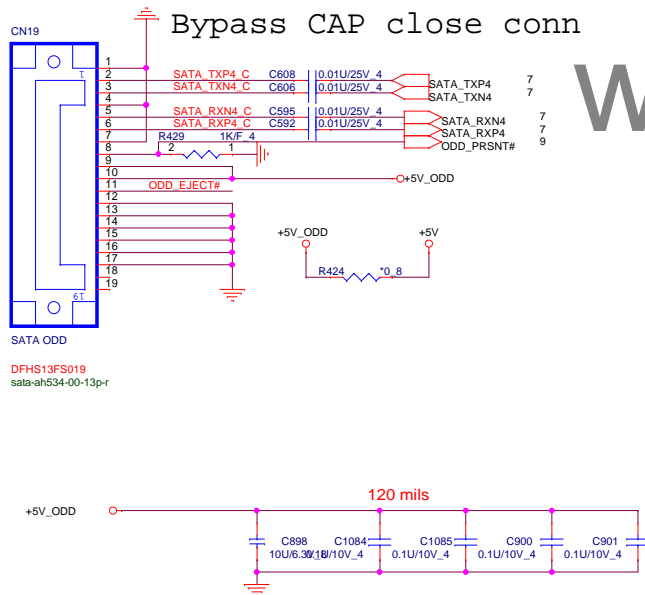


SATA HDD CONNECTOR

32

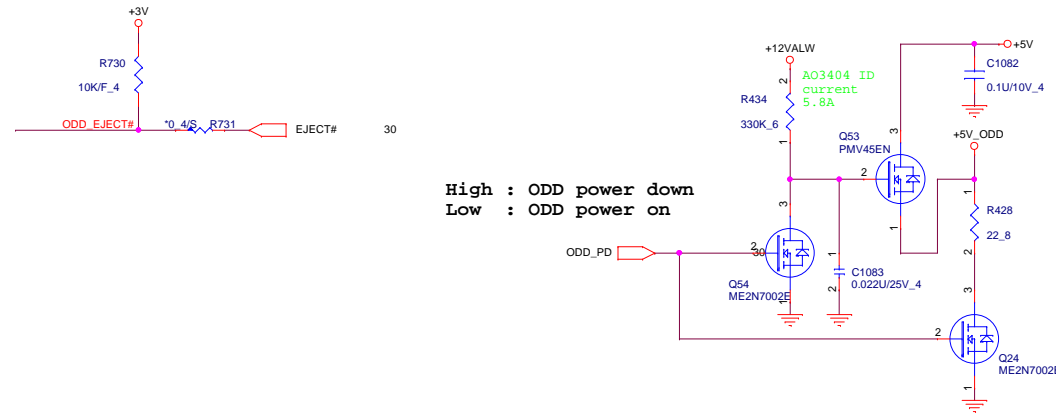


SATA ODD CONNECTOR



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follow INTEL DG change eject PU to +3V.

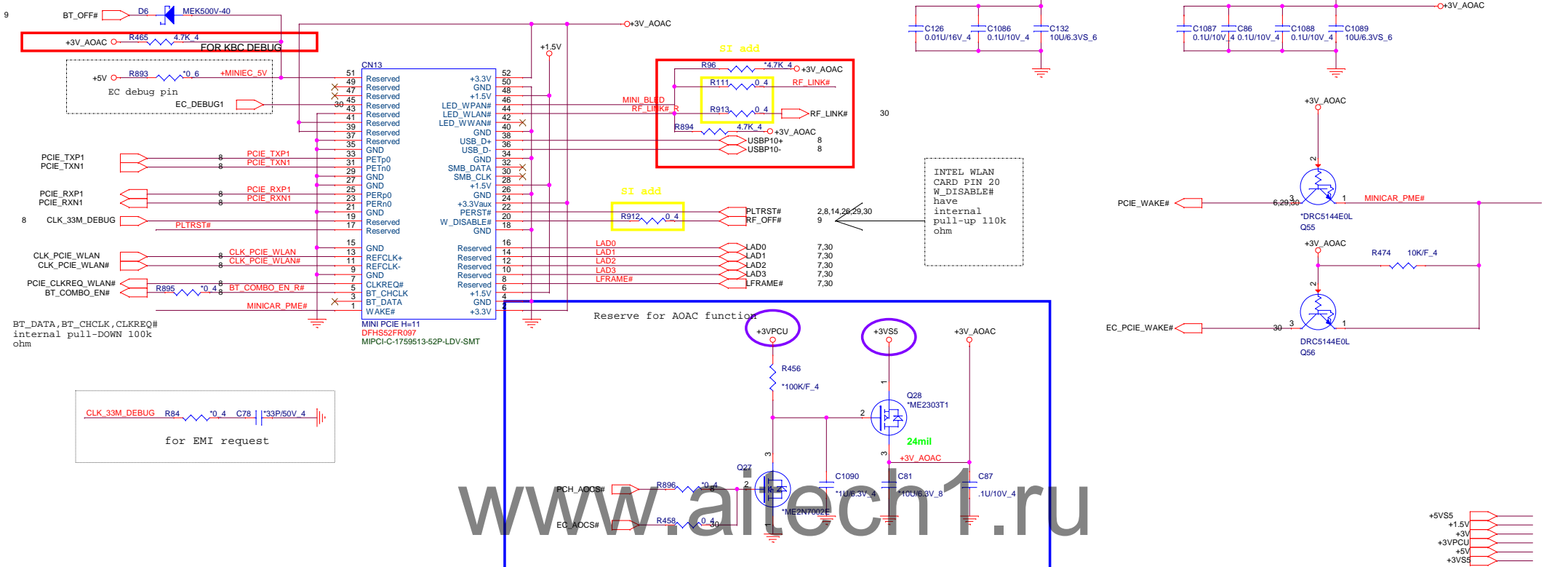


+3V
+3VPCU
+5V
+12VALW

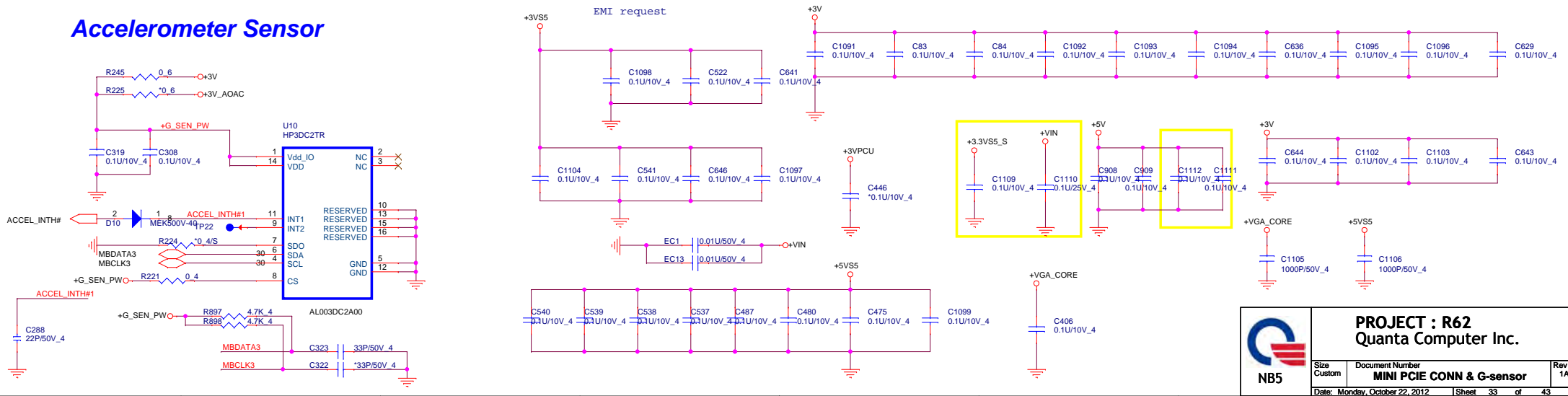
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5,7,25,30,31,33,34,35
7,10,23,25,27,31,33,39
34,39,43

Mini PCI-E Card 1 WLAN

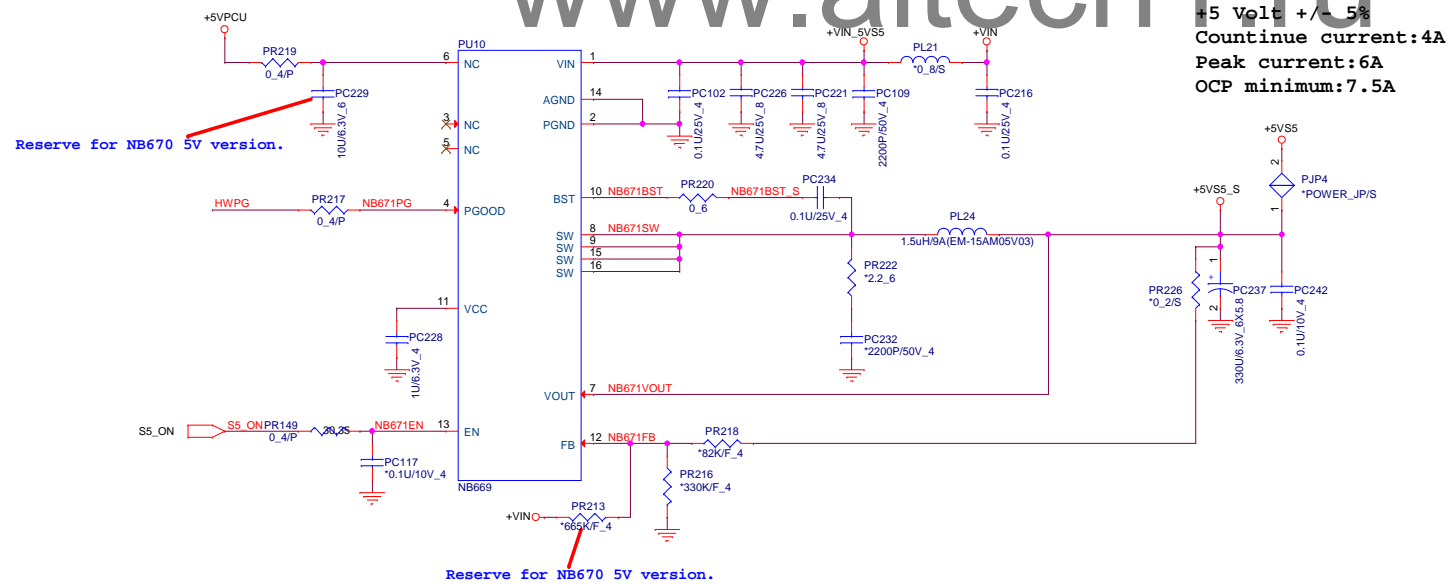
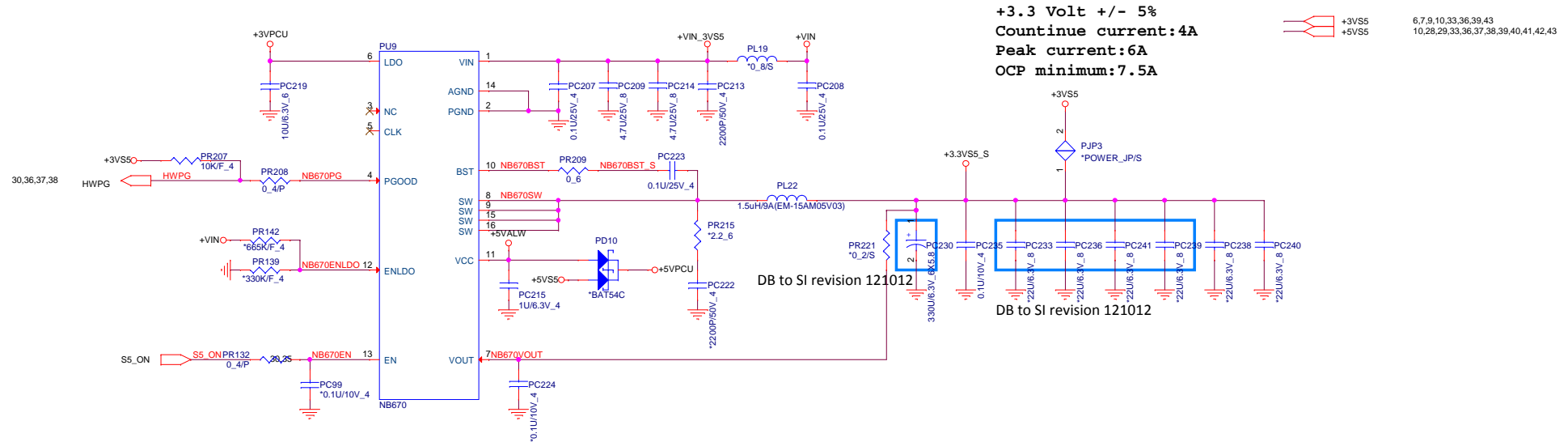
33

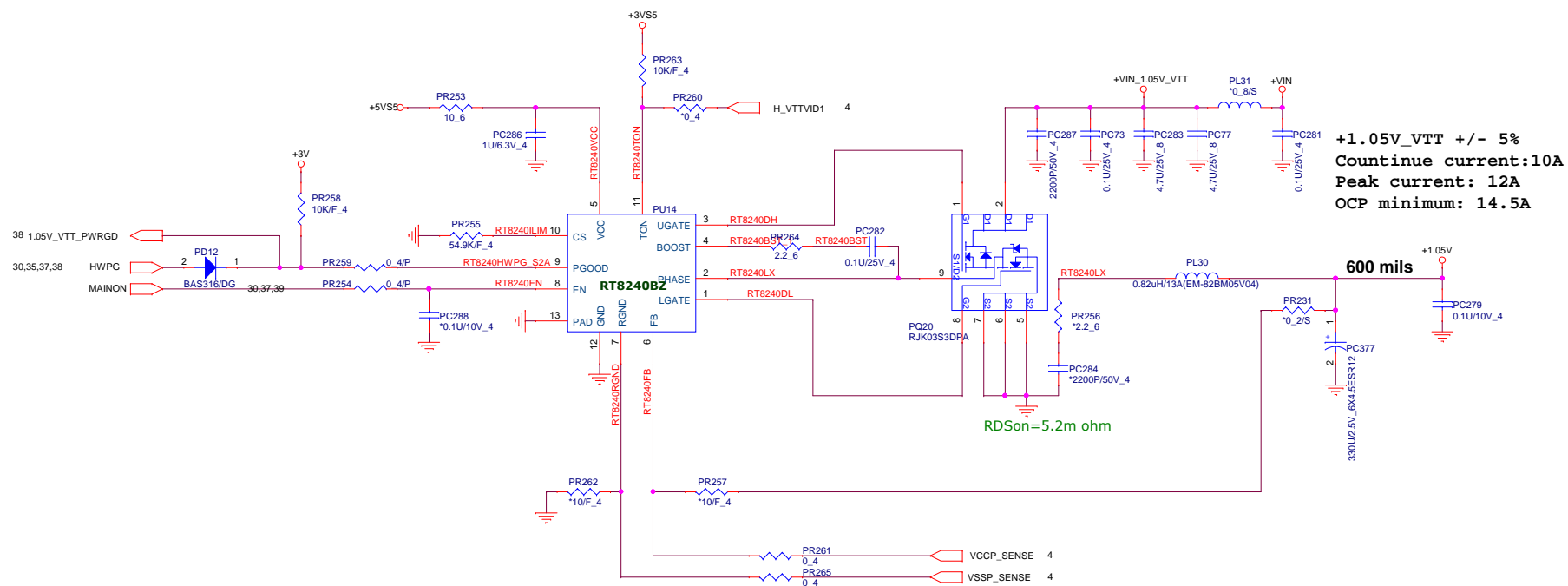


Accelerometer Sensor

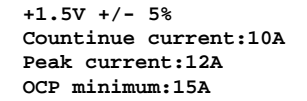




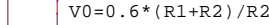




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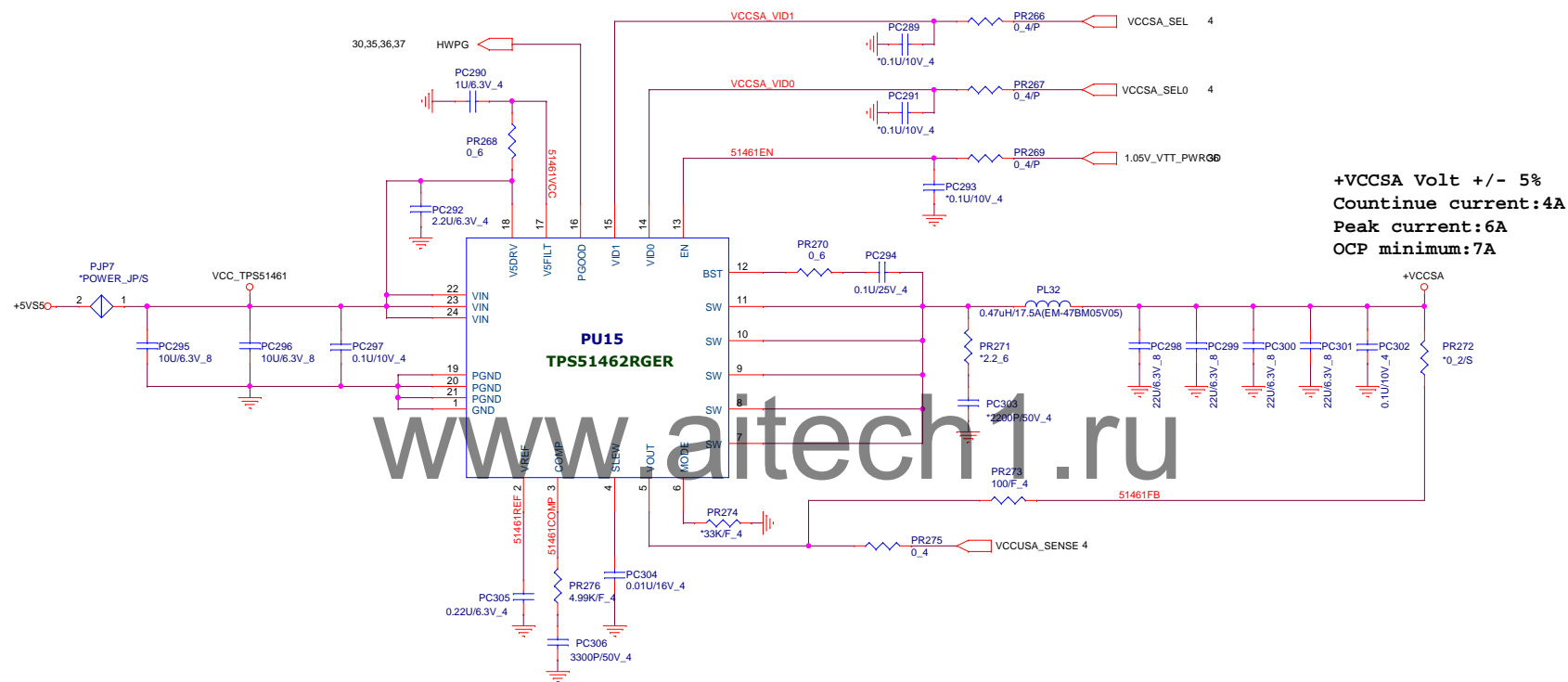
1.8V +/- 3%
Continue current:2A
Peak current:3A
OCP minimum:4A

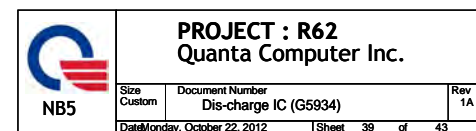


TPSS1462RGER/AL051462000

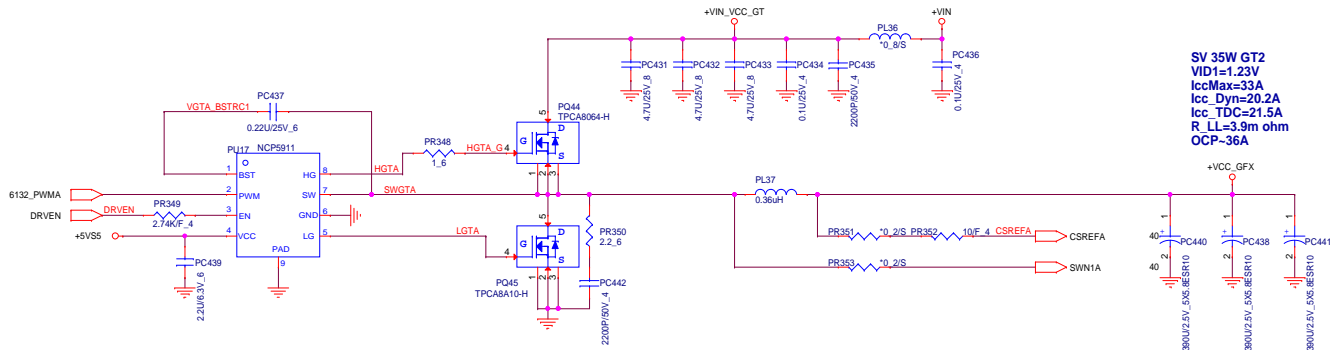
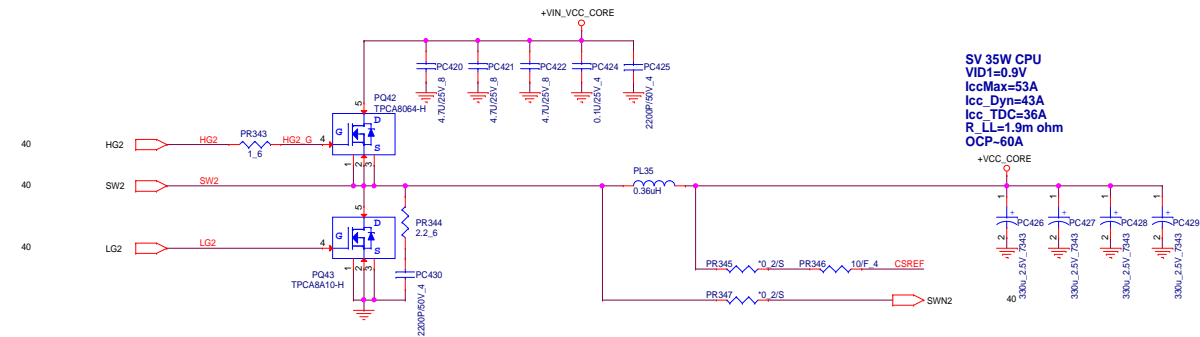
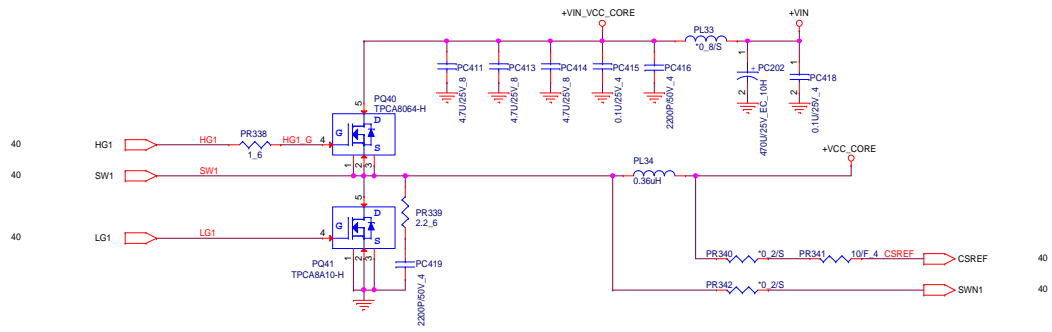
For CPU SV system agent
voltage slew rate of 0.5 -10 mV/ μ s

SEL0	SEL1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V



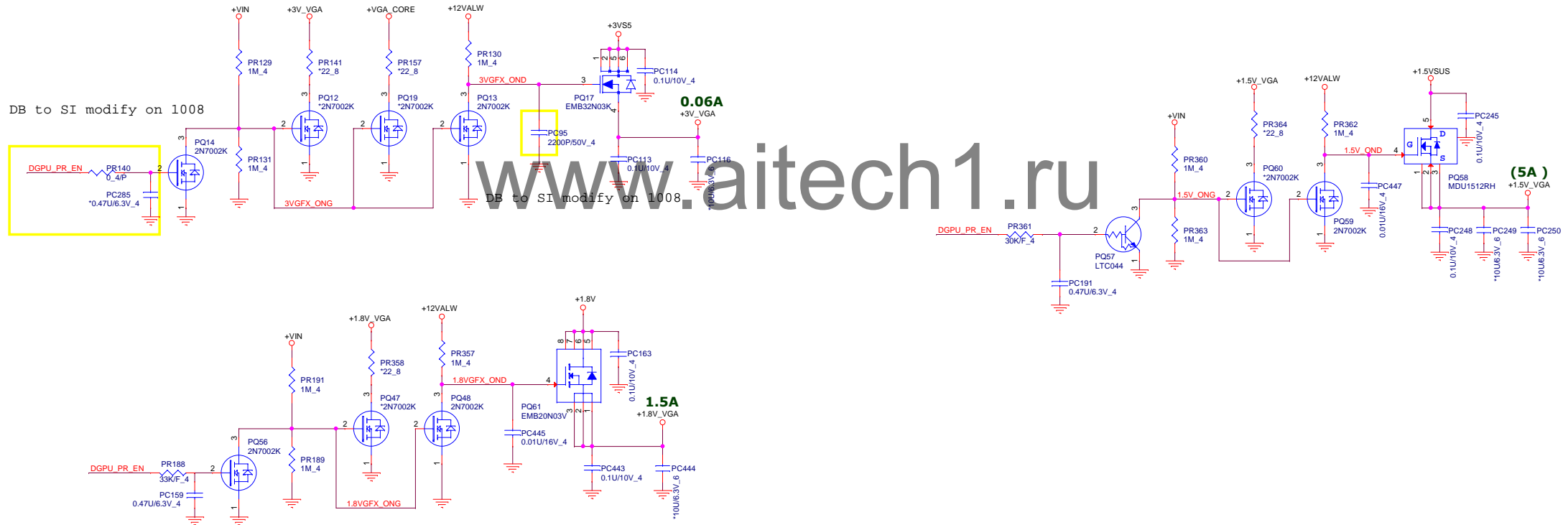
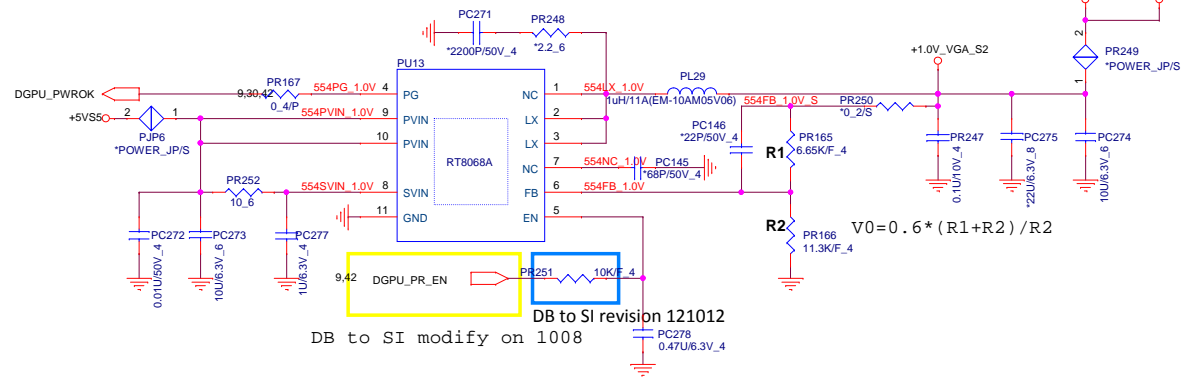






R2 Value	P/N	1.0V_VGA
10K	CS31002FB26	1.0V
11.3K	CS31132FB07	0.95V

+0.95V +/- 3%
 Countinue current:2A
 Peak current:3A
 OCP minimum:4A



+1.8V_VGA 15,16,18,19,25
 +1.0V_VGA 14,16,18,19
 +3V_VGA 18